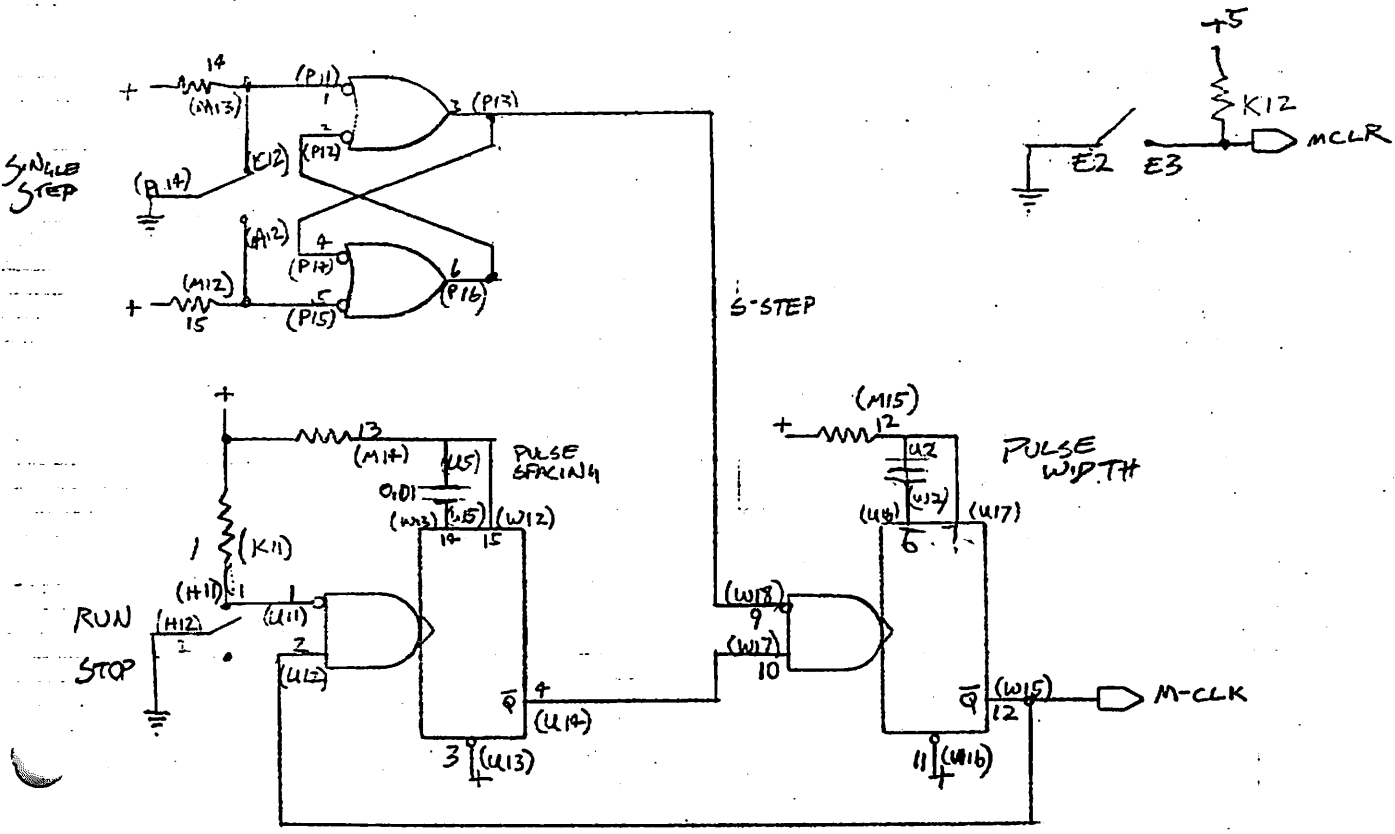
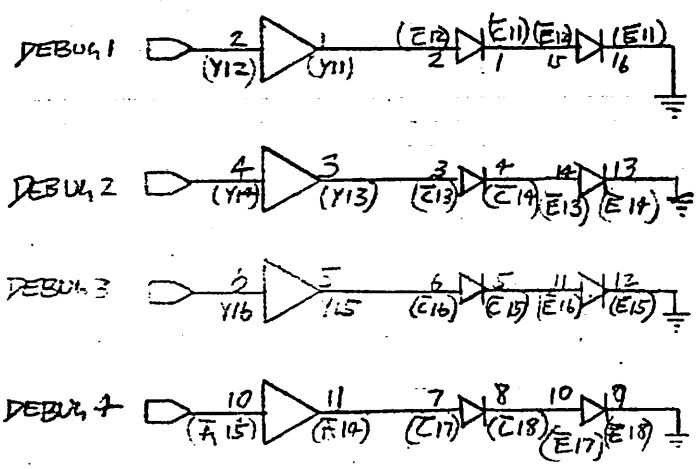
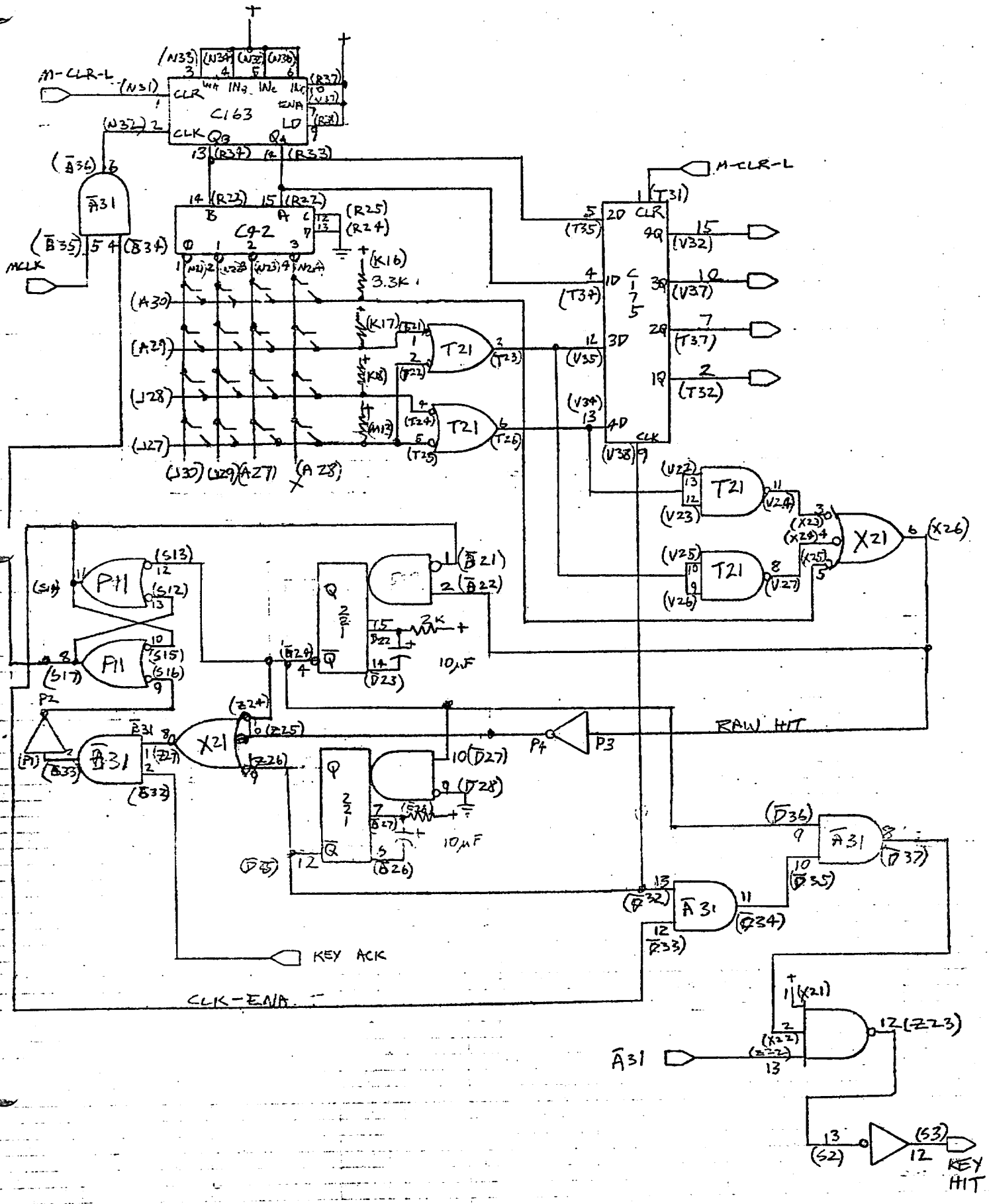
CLOCK CIRCUIT FOR CALCULATOR (LAB 6)

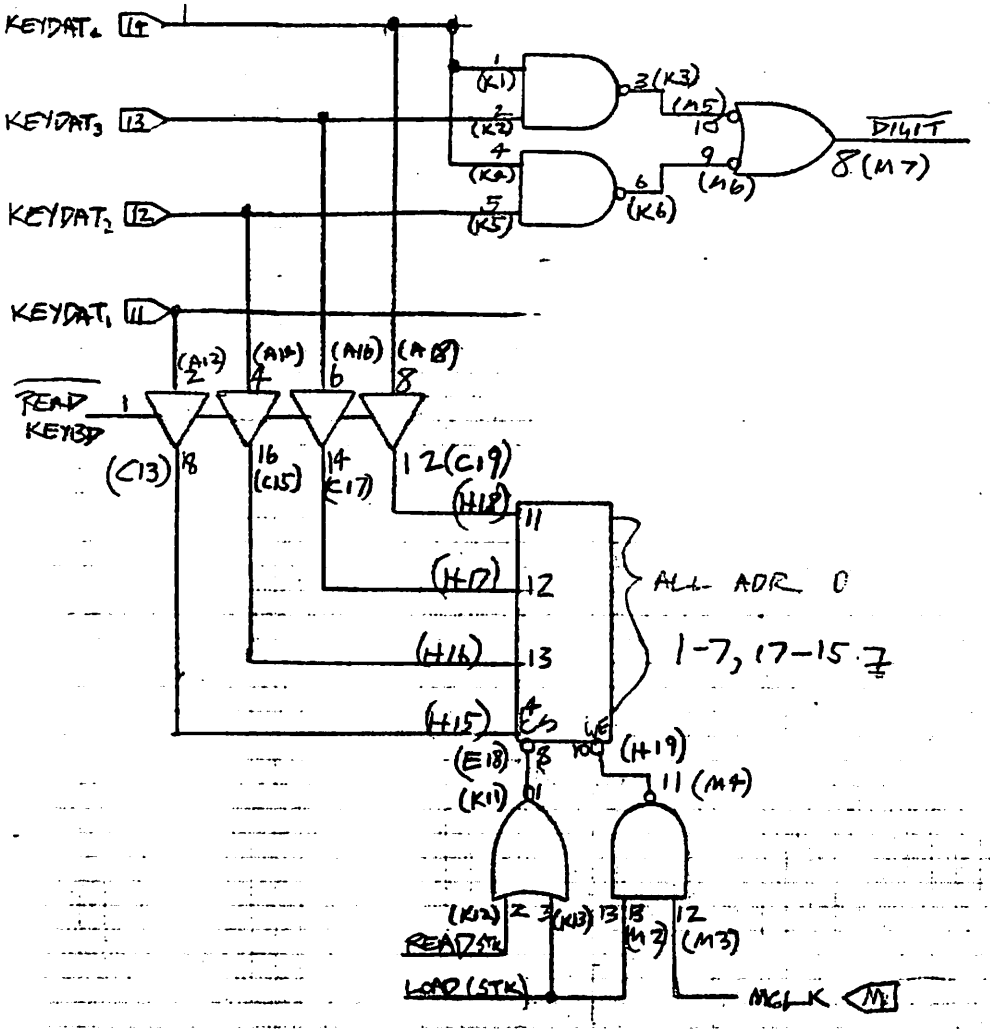




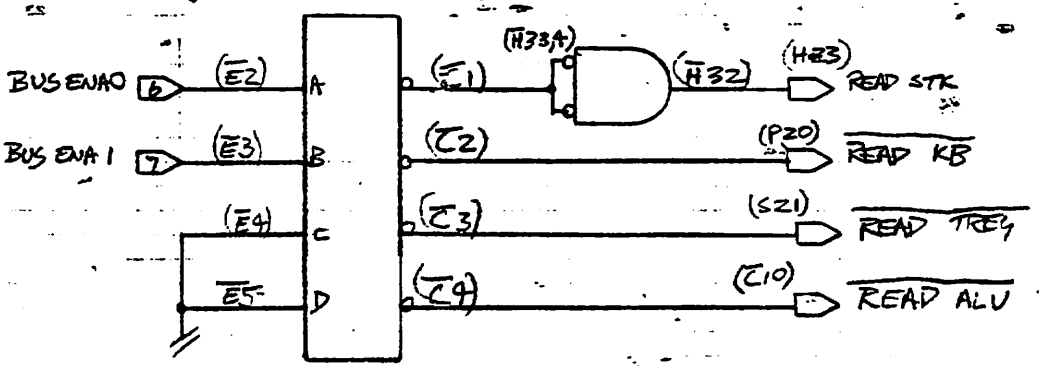
KEYBOARD DECODER & DEBOUNCER FOR CALCULATOR

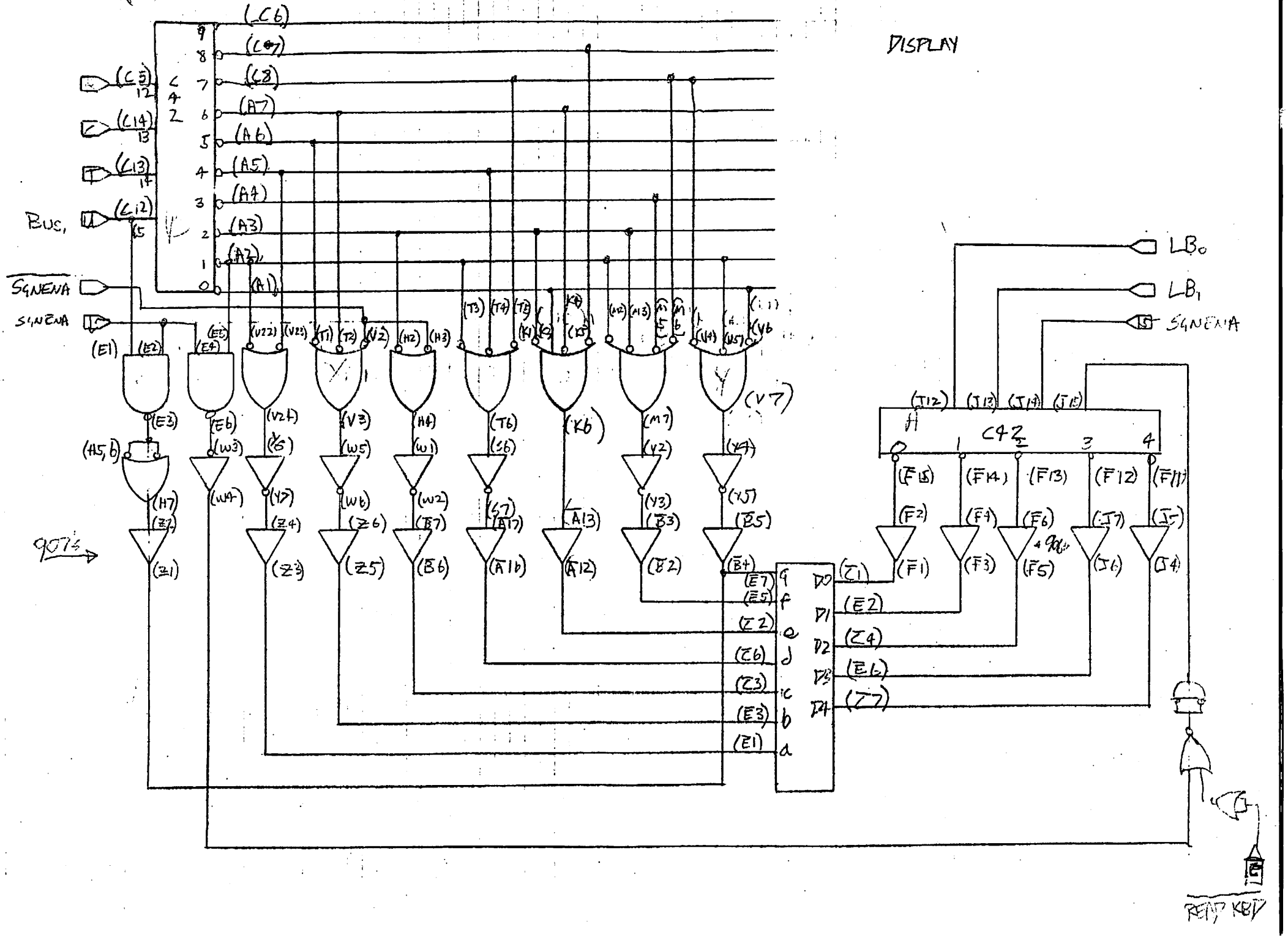


DEMO RAM CIRCUIT FOR WED. CHKPOINT
(NOW TORN APART)

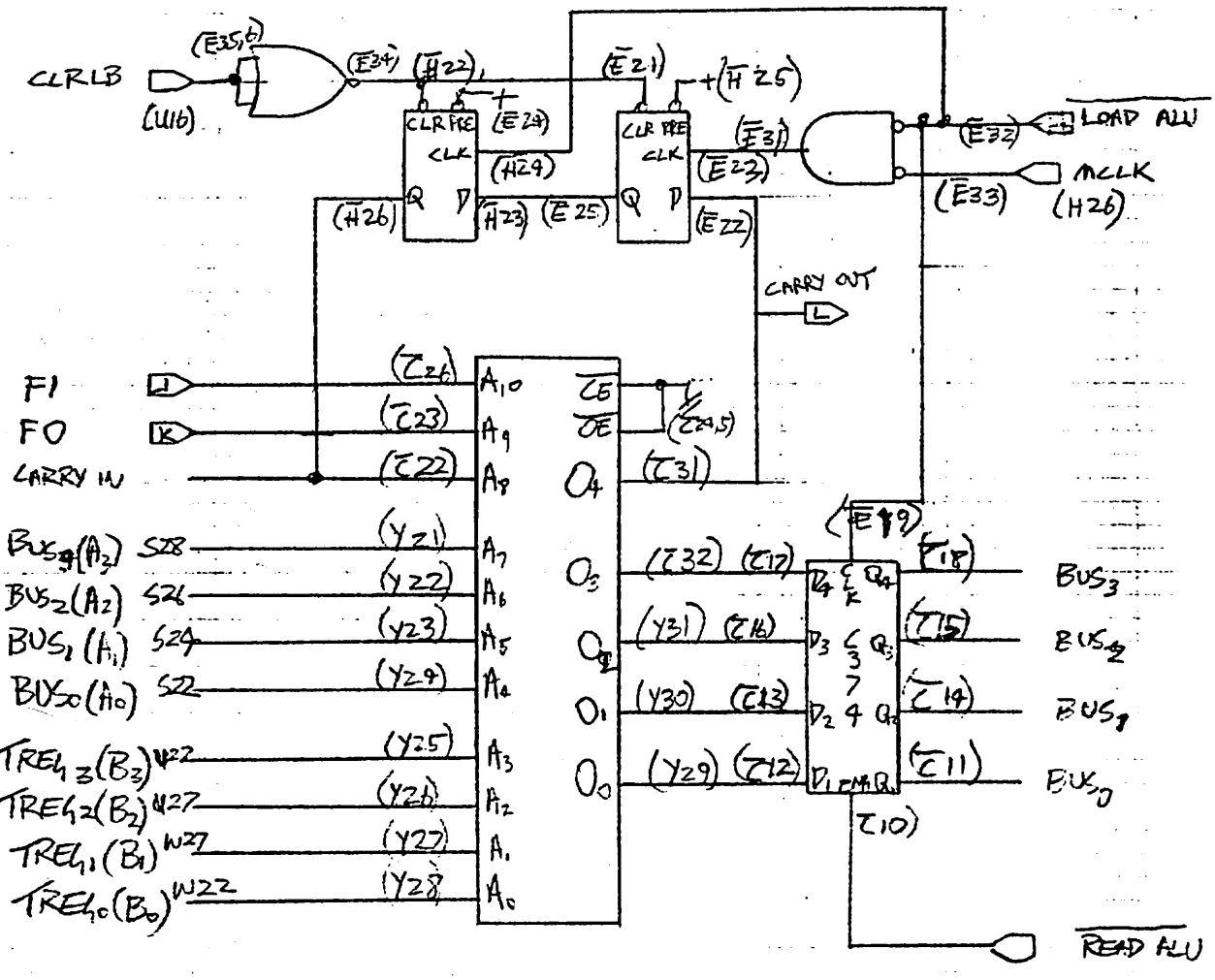


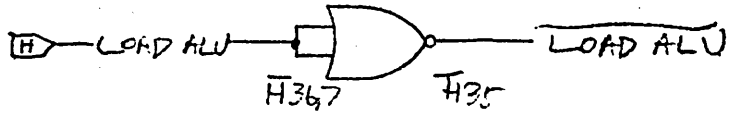
BUS READ CONTROL LINE CHANGE

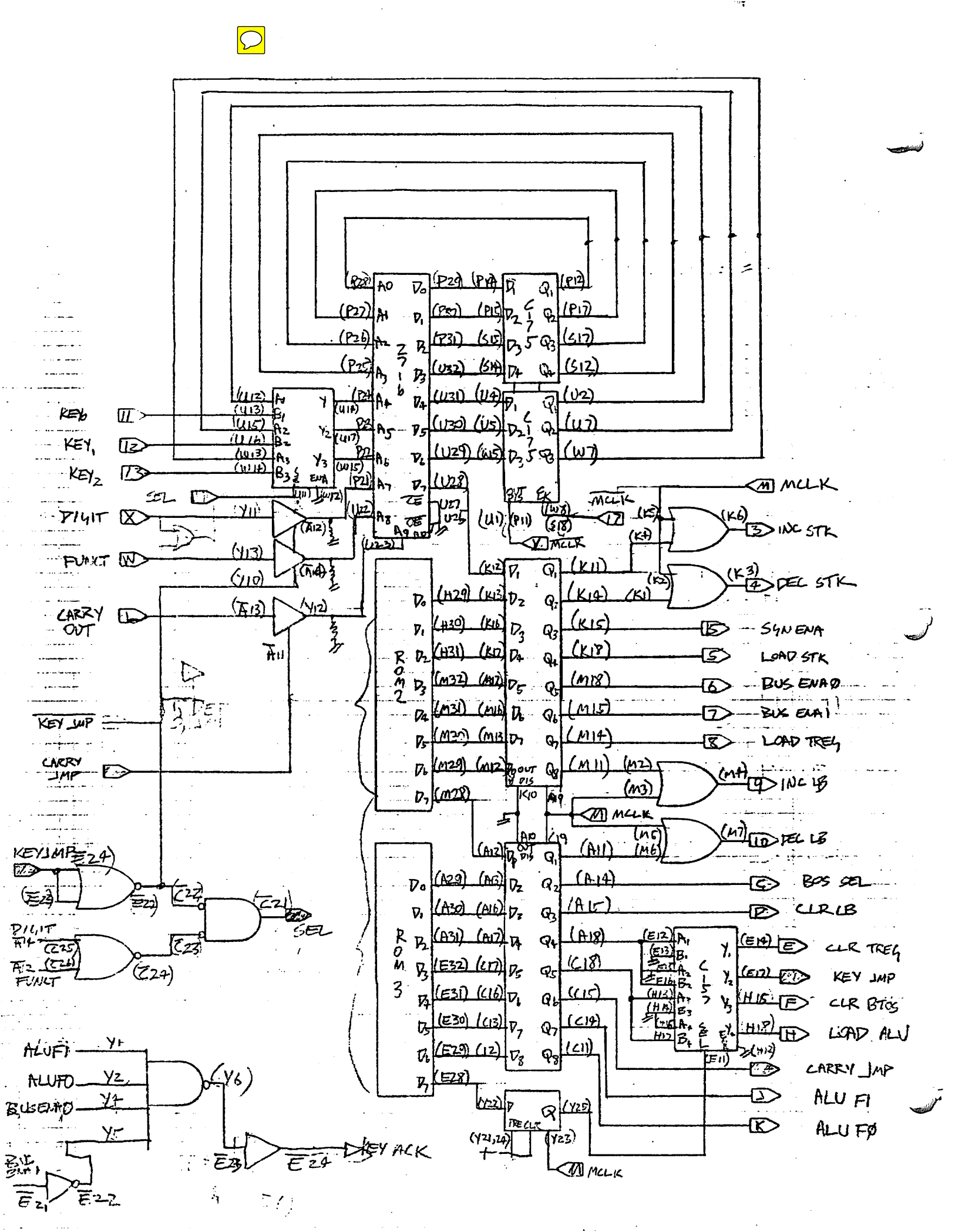



DISPLAY
BUS,
SGNENA
SGNENA
LB0
LB1
SGNENA
C42
C42
READ KBD

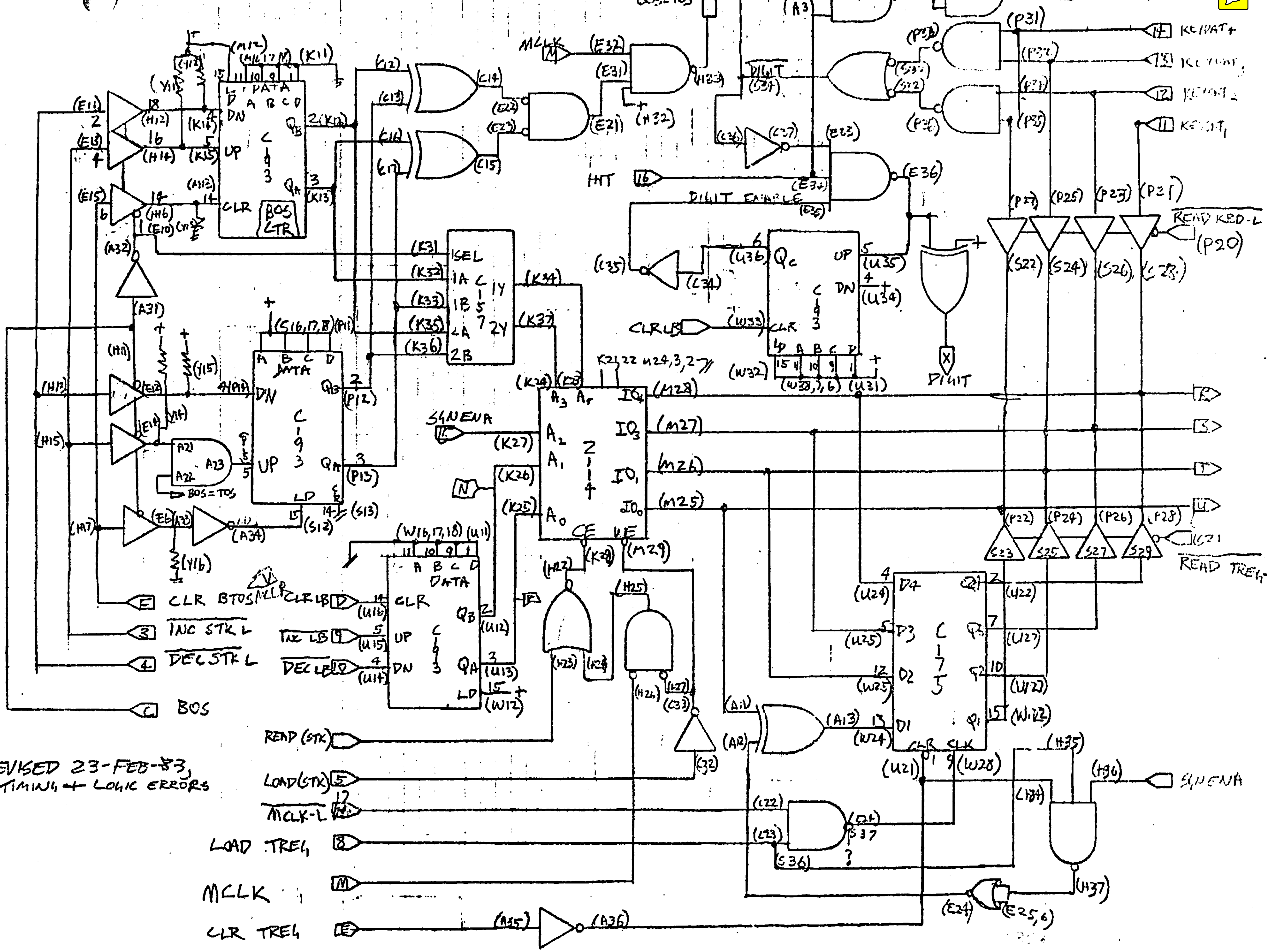
CALCULATOR
ALU 25-FEB-83



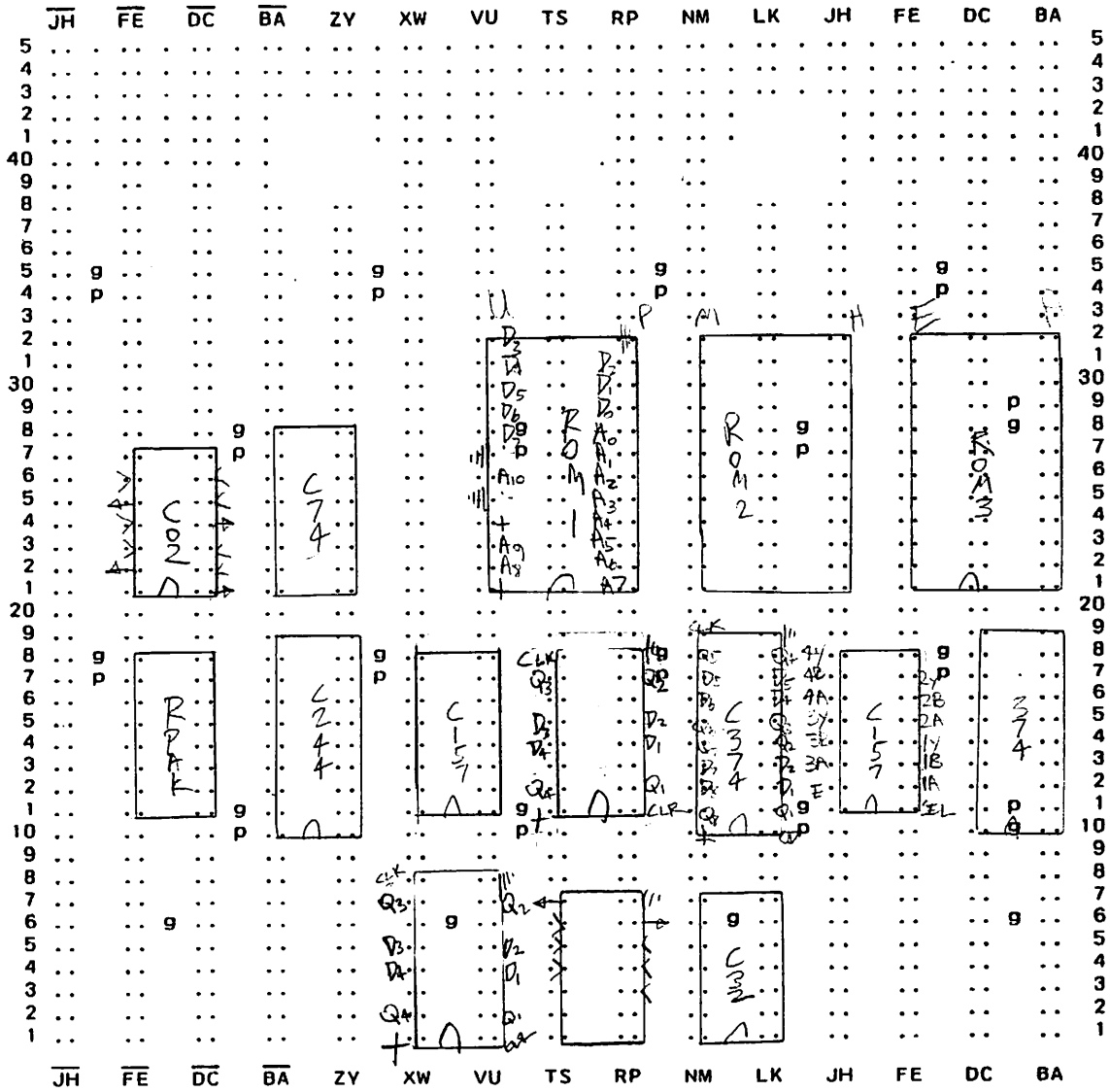



KEY0
KEY1
KEY2
SEL
DIGIT
FUNCT
CARRY OUT
KEY JMP
CARRY JMP
MCLK
INC STK
DEC STK
SYN ENA
LOAD STK
BUS ENA0
BUS ENA1
LOAD TREG
INC LB
DEC LB
BUS SEL
CLR LB
CLR TREG
KEY JMP
CLR BTCS
LOAD ALU
CARRY_JMP
ALU F1
ALU F0
ROM 2
ROM 3
Z7168
C175
ALUF1
ALUF0
BUSENA0
KEY ACK

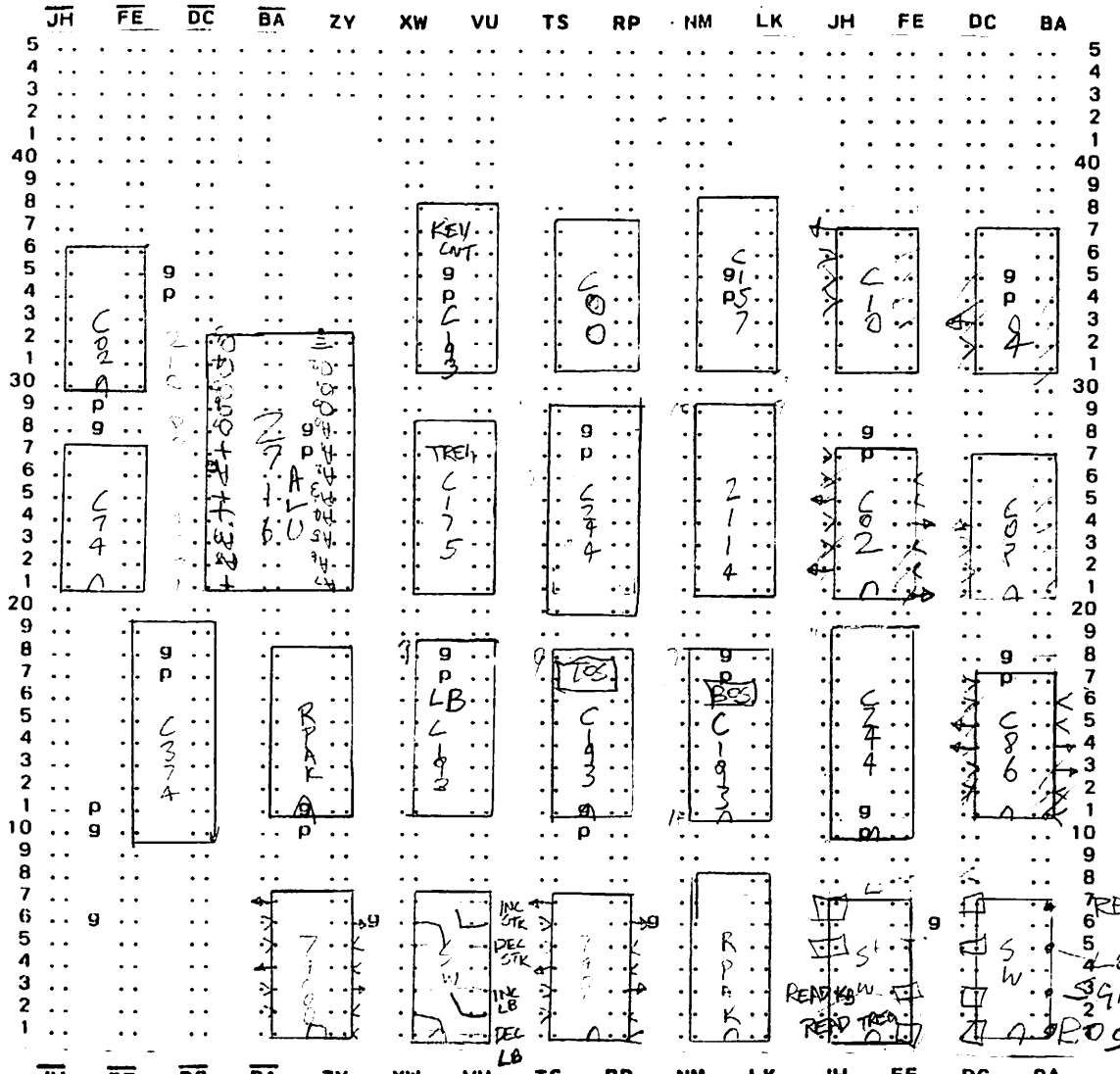
CALCULATOR-STACK DESIGN



REVISED 23-FEB-83, TIMING + LOGIC ERRORS



LAYOUT FOR STATE MACHINE



STACK & ALU LAYOUT

DEBUG SWITCHES

YB / A12 / A13 / F14	INC STK DEC STK INC LB DEC LB	LD TREG CLR LB BUS EXT BUS ENB	READ STK LD CTK ALU ENA EOS

"ON"

F1
F0
WRK ALU
RD ALU

ON

F0
F1

LAYOUT FOR CLOCK & KEYBOARD