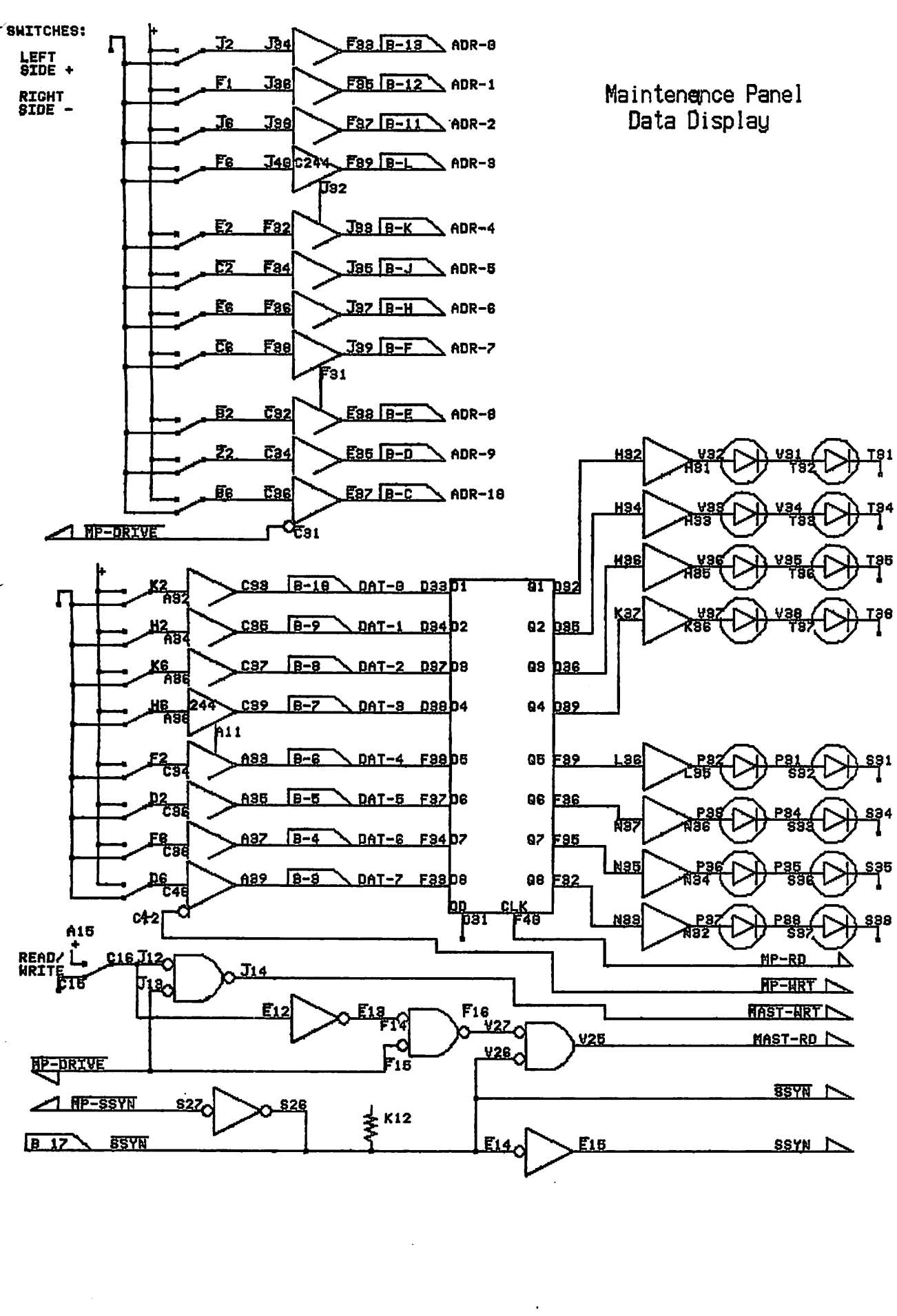
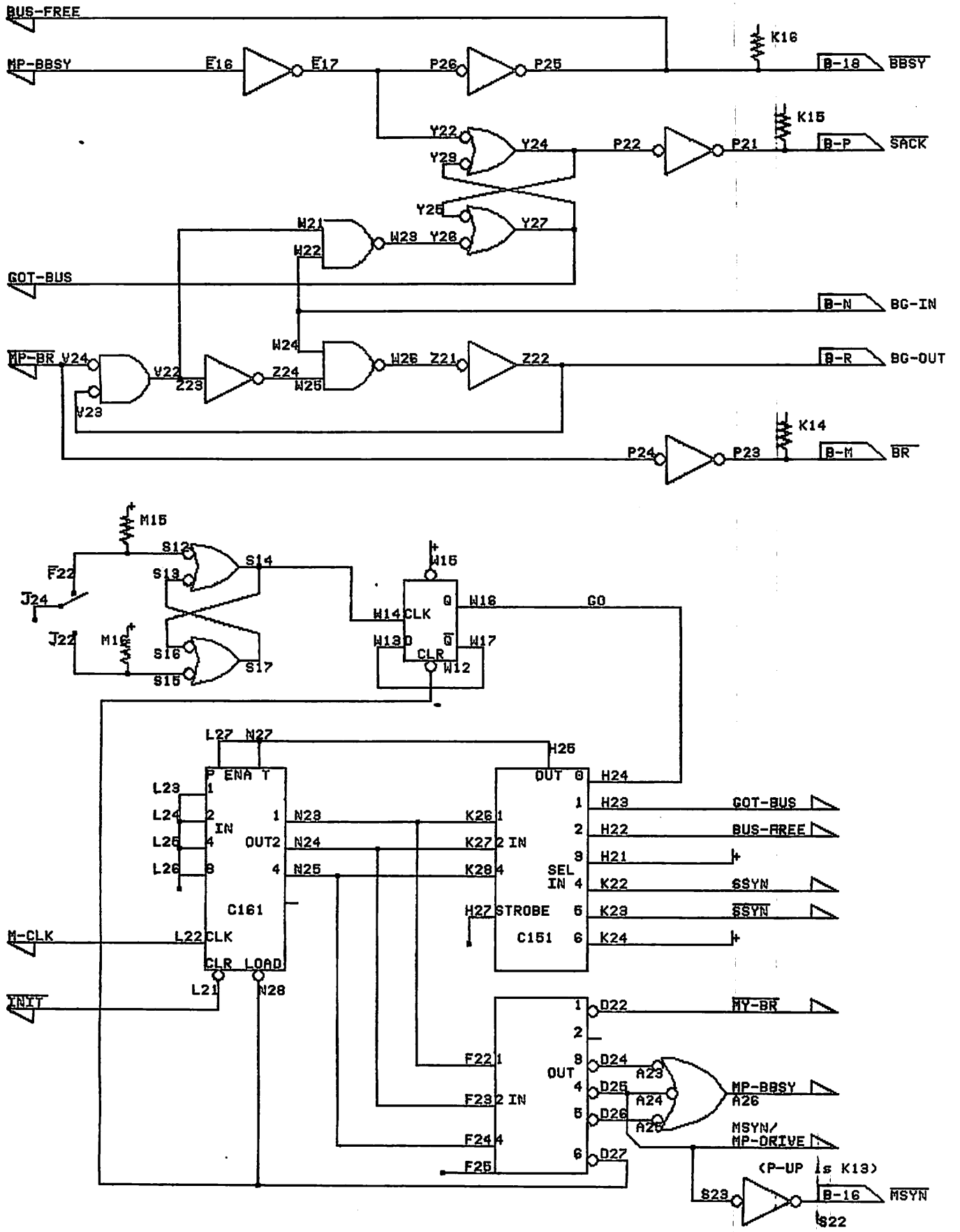
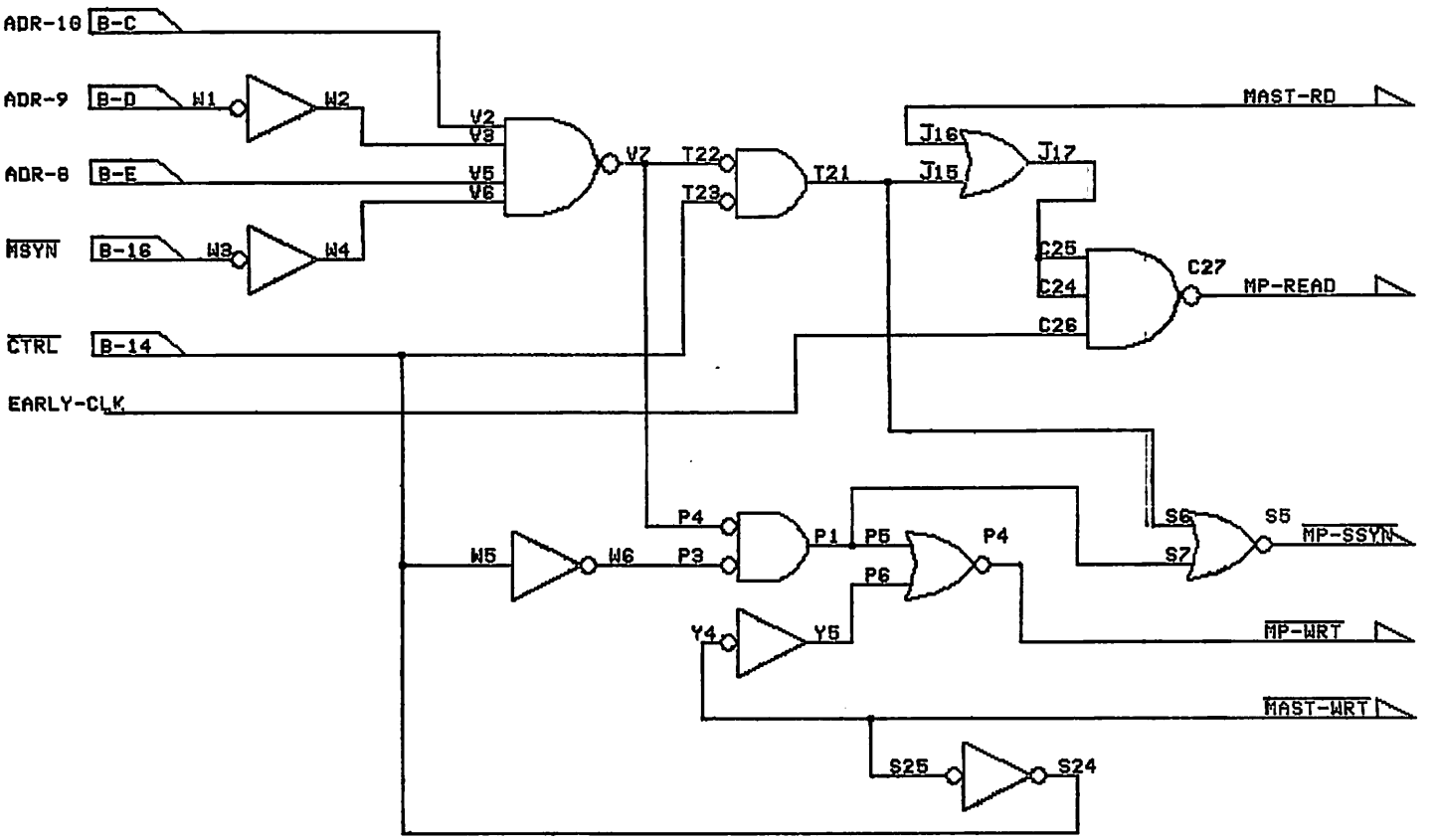
Maintenance Panel Data Display



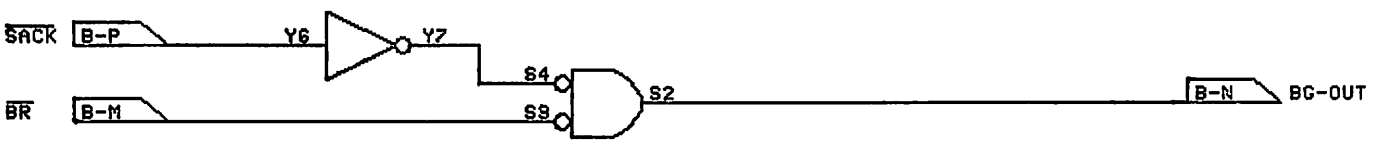
Maintenence Panel - Control



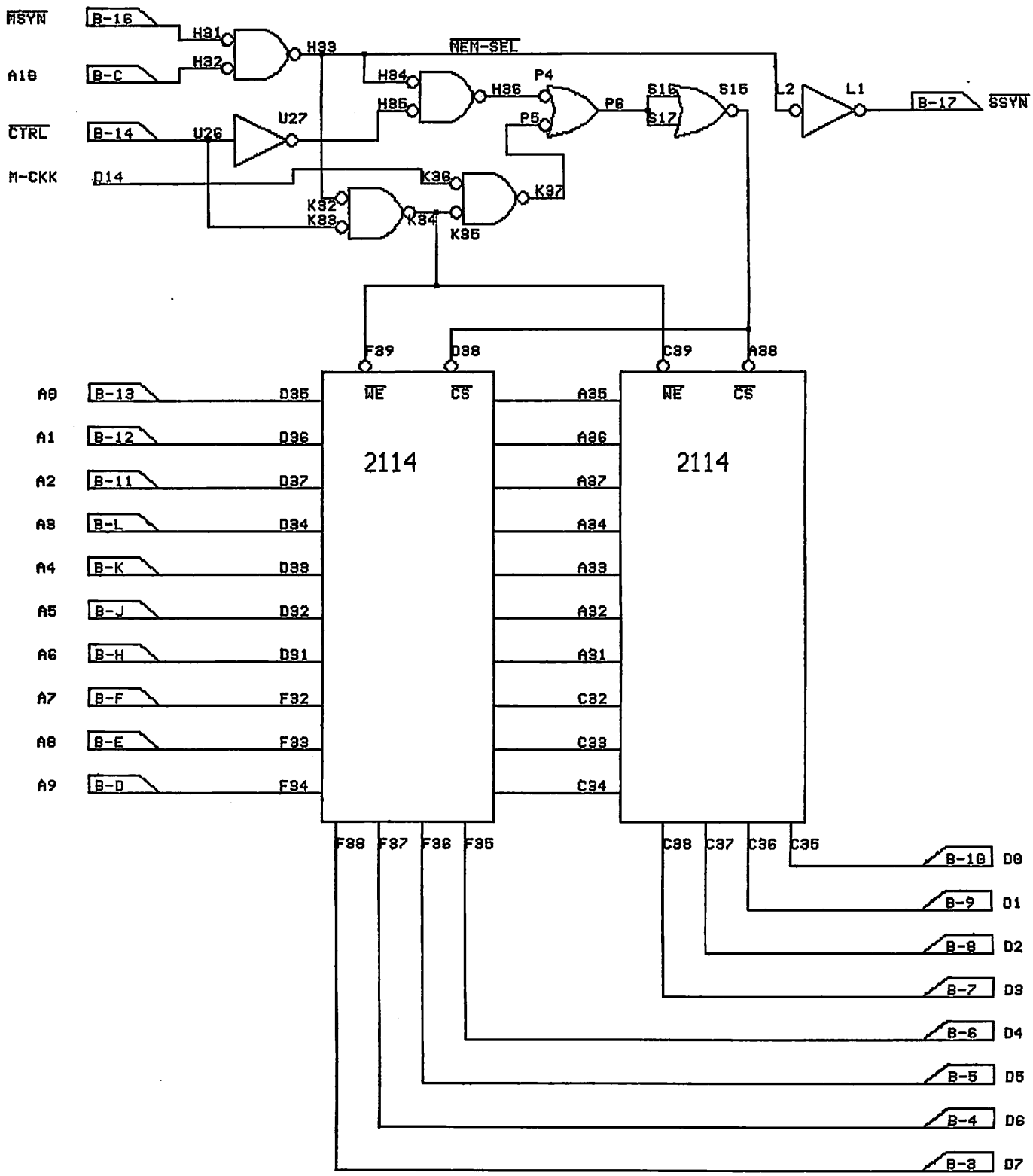
Maintenence Panel
Slave Logic

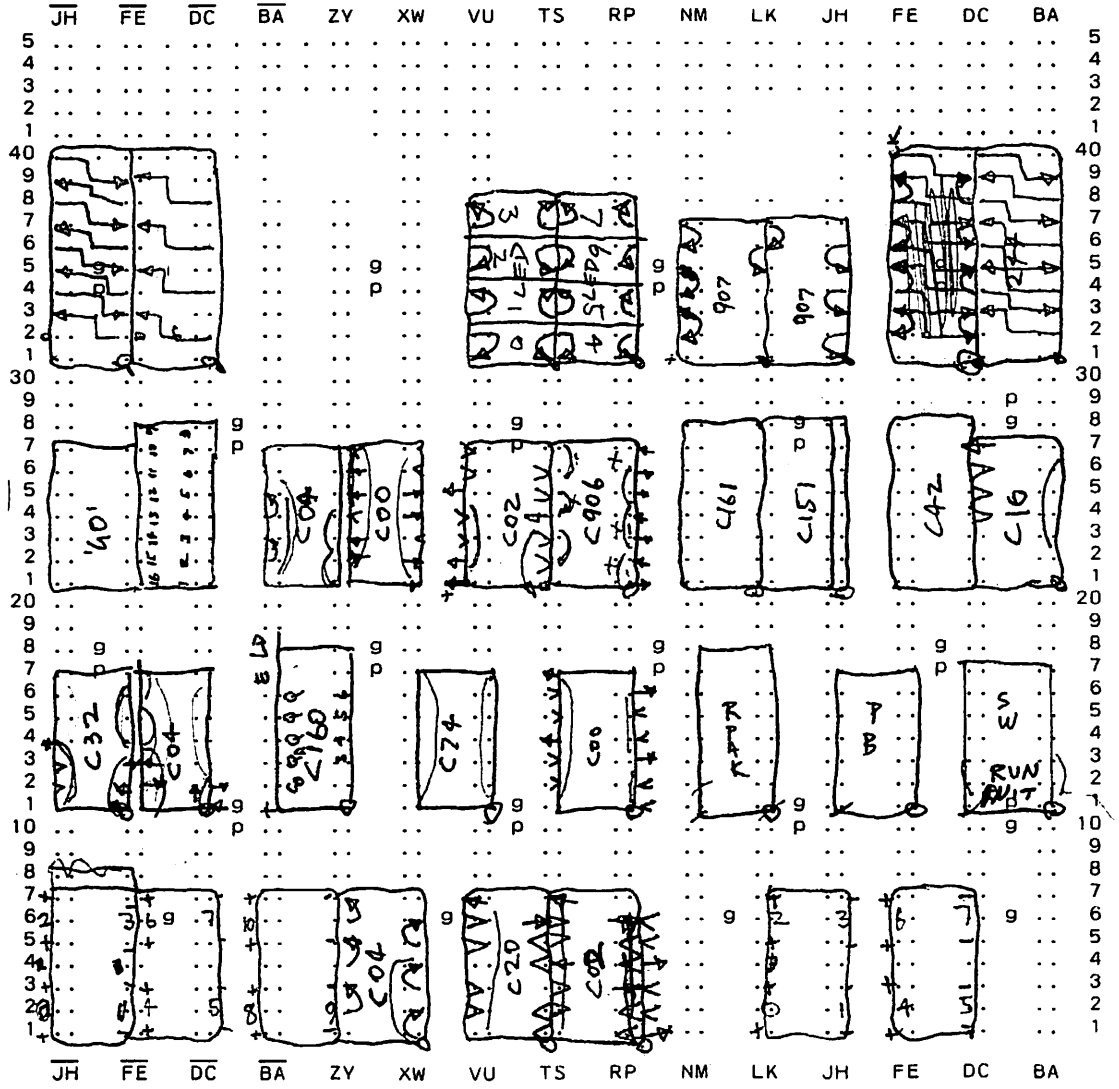


Bus Arbitration Logic



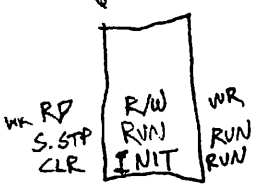
1K Memory System





MAINTENENCE PANEL &

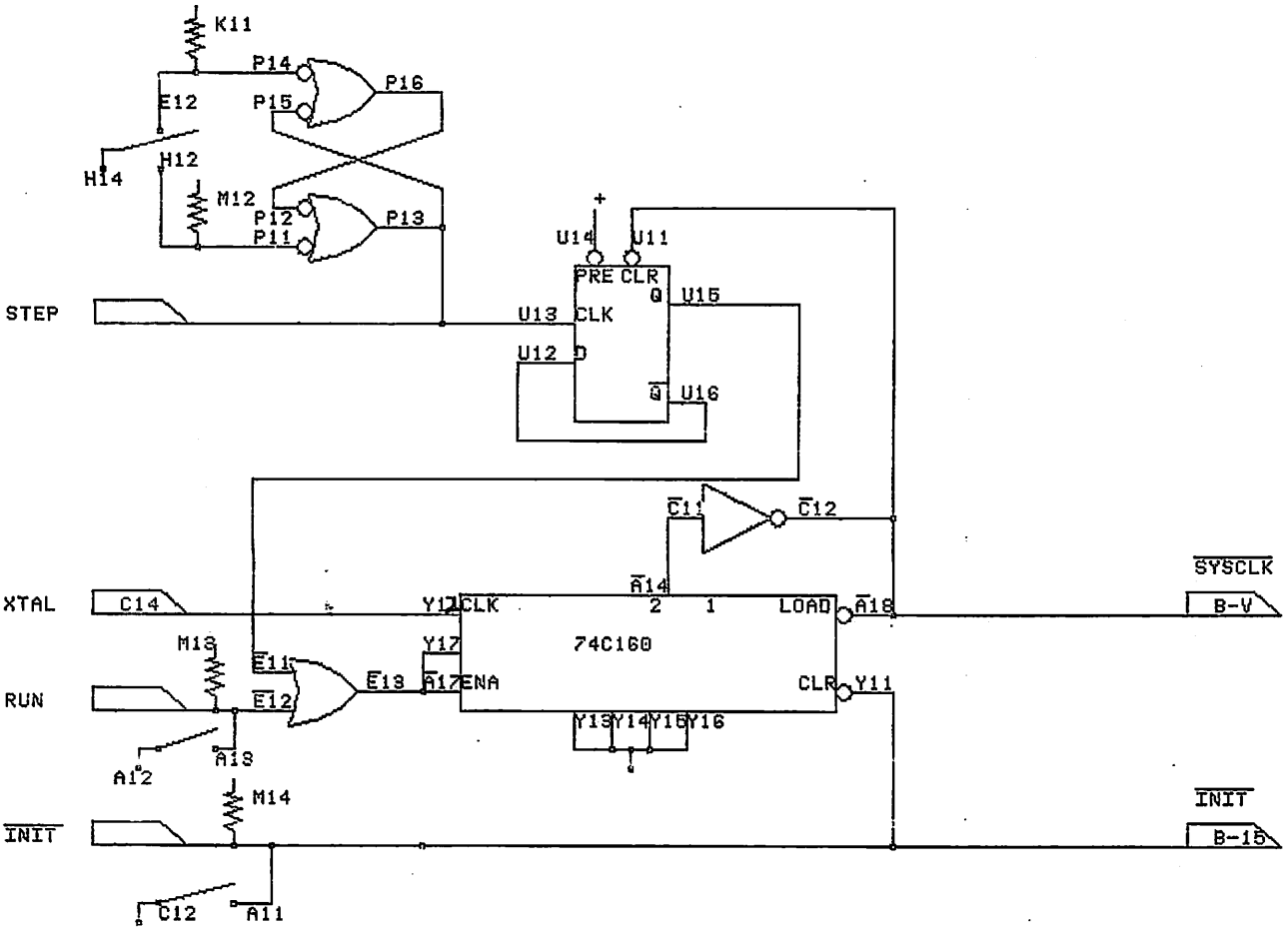
CLOCK
LAYOUT



D	C	B	A	Z	Y	X	W	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C
2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3
6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0							

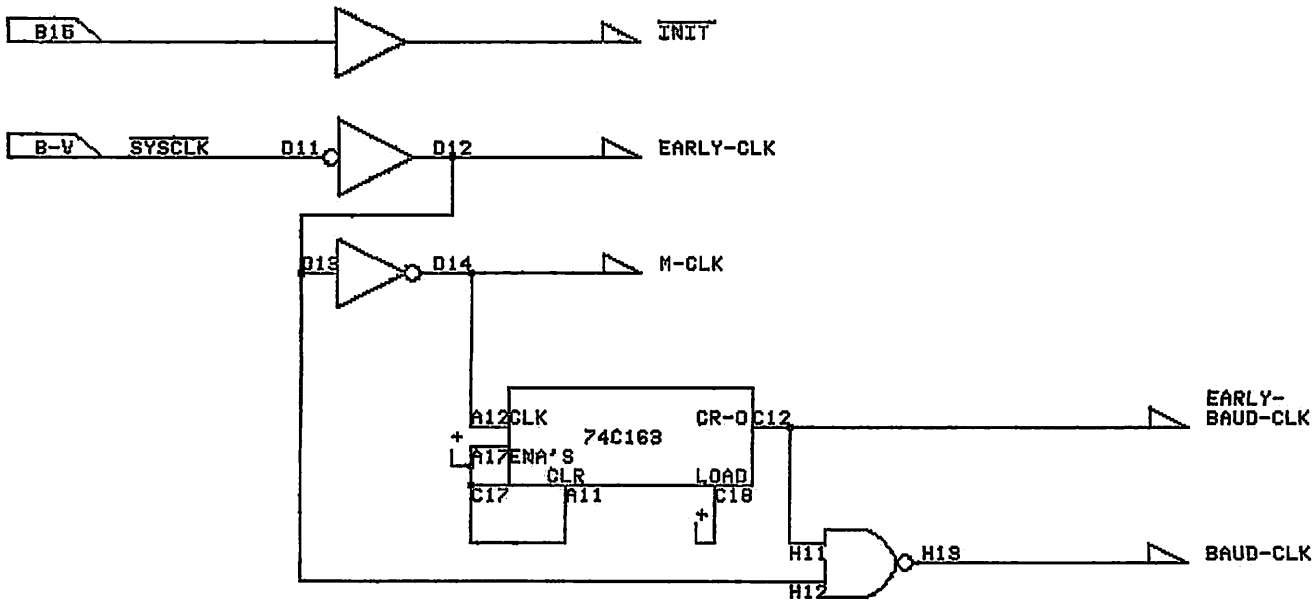
CHIP SIDE

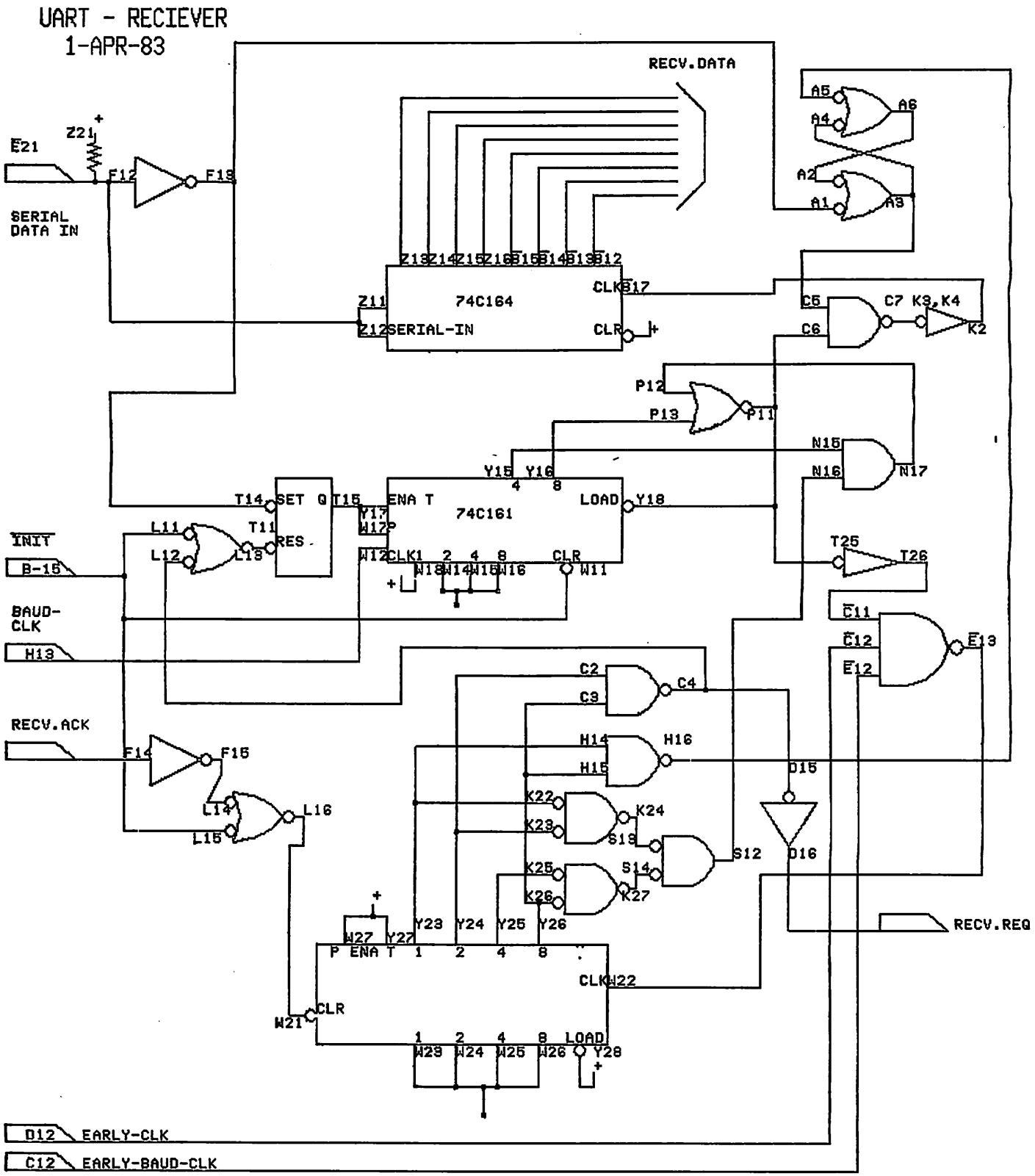
System Clock
3-APR-83



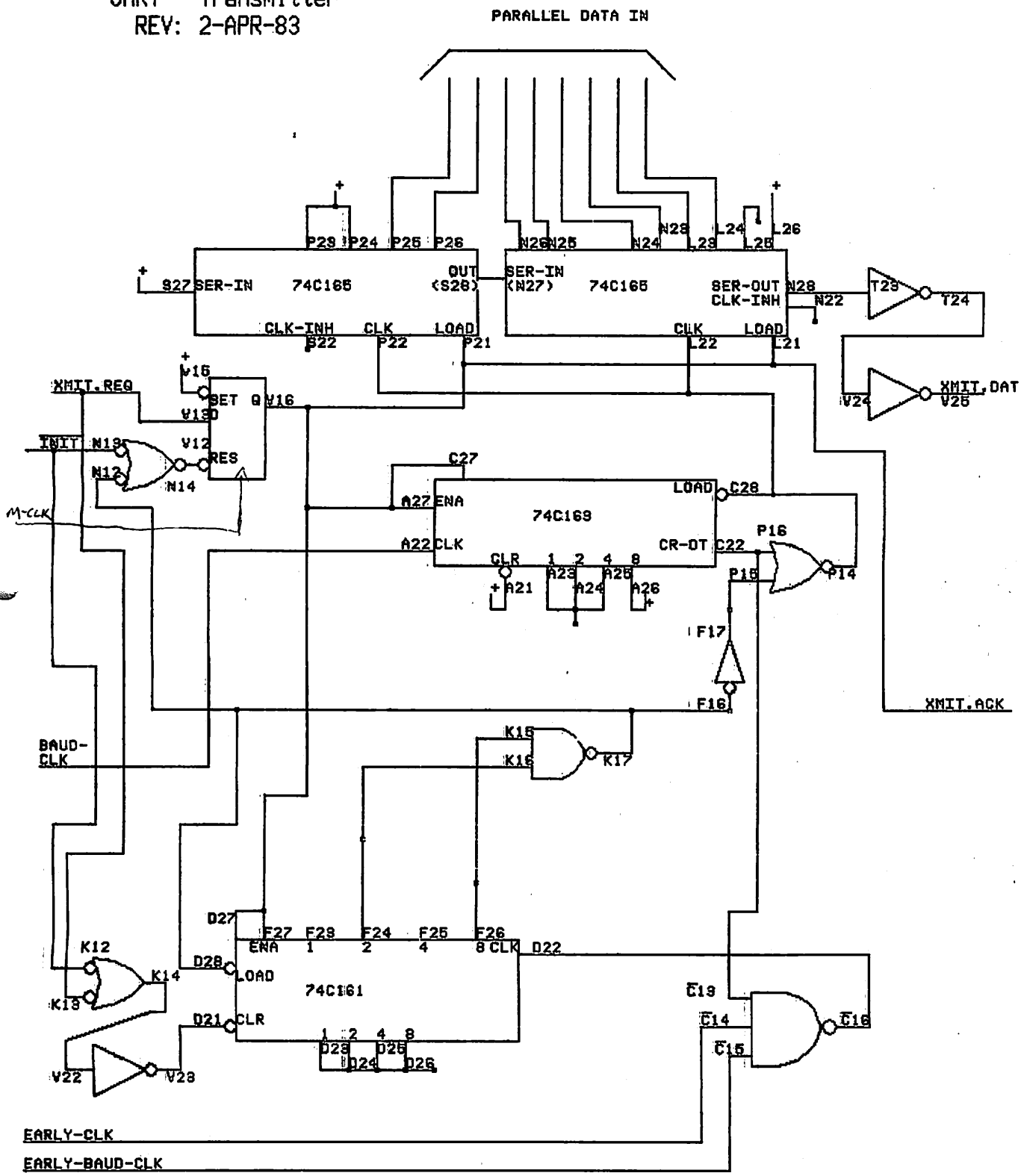
Bus Interface for UART (clock)

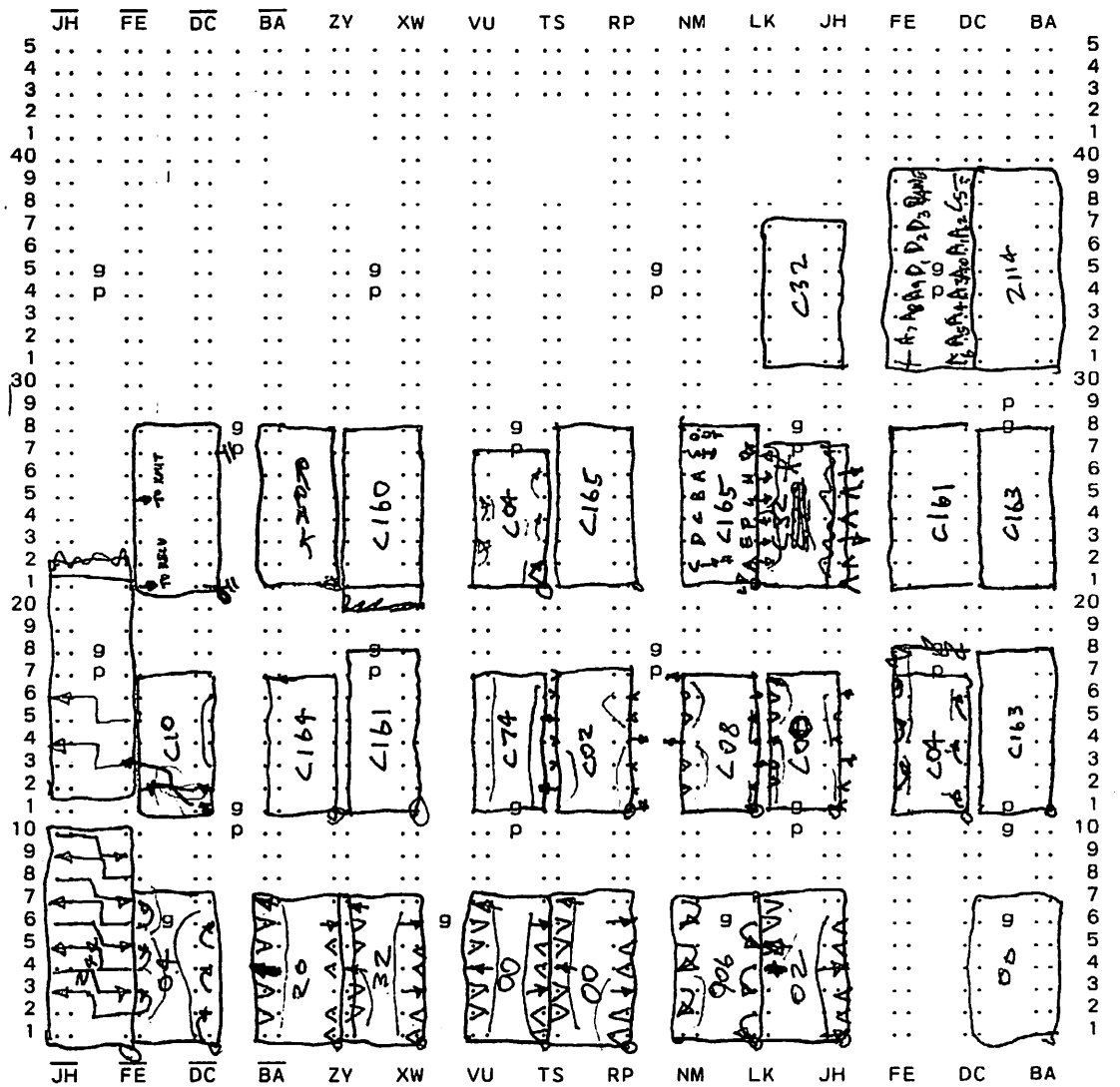
2-APR-83




UART - RECIEVER
1-APR-83
RECV.DATA
E21
Z21
F12
F13
SERIAL
DATA IN
74C164
SERIAL-IN
CLK
CLR
74C161
ENA T
LOAD
SET Q
RES
INIT
B-15
BAUD-
CLK
H13
RECV.ACK
F14
F15
L16
RECV.REQ
D12 EARLY-CLK
C12 EARLY-BAUD-CLK

UART - Transmitter
REV: 2-APR-83





D C B A Z Y X W V U T S R P N M L K J H F E D C

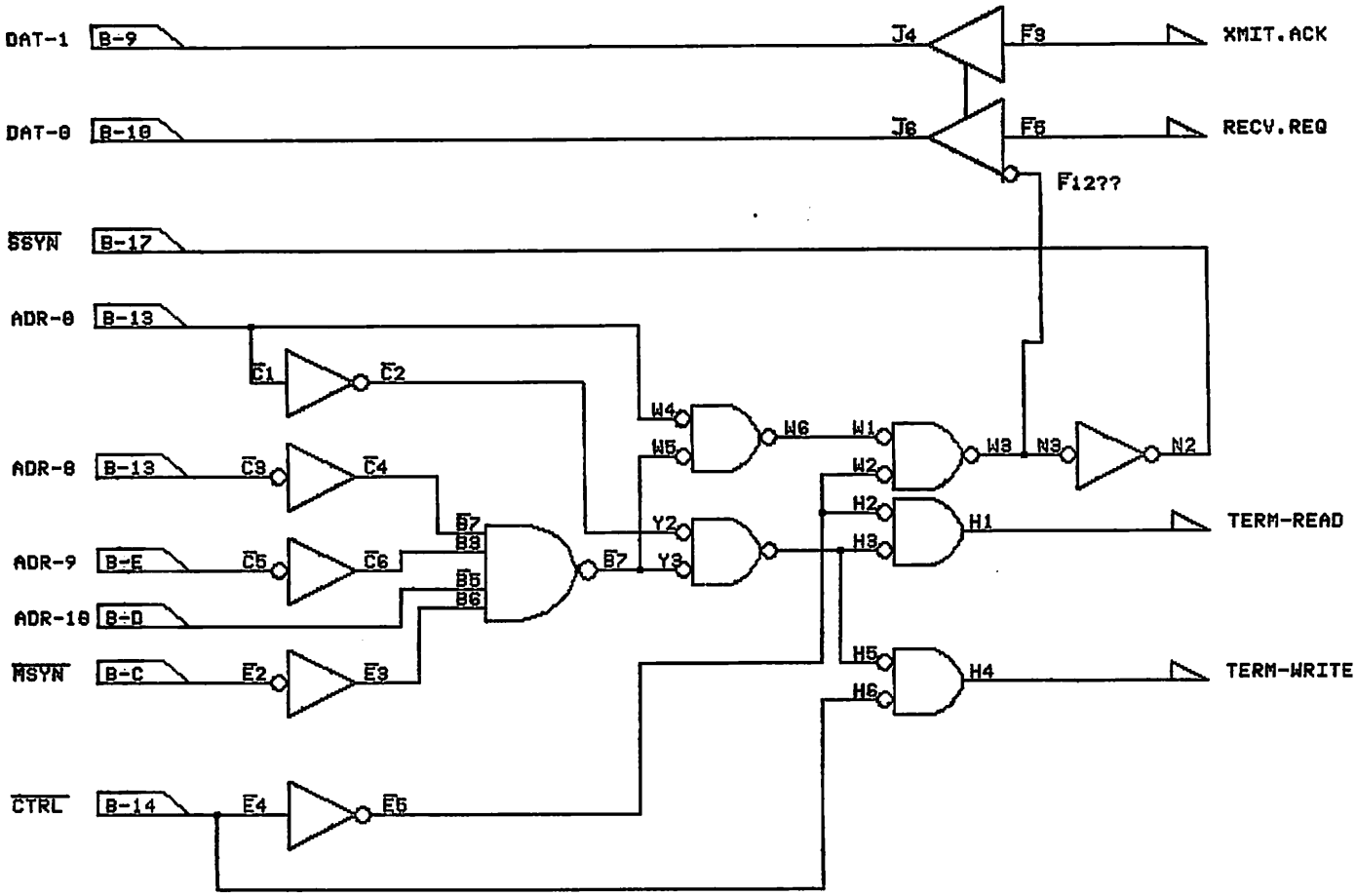
2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3
6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

CHIP SIDE

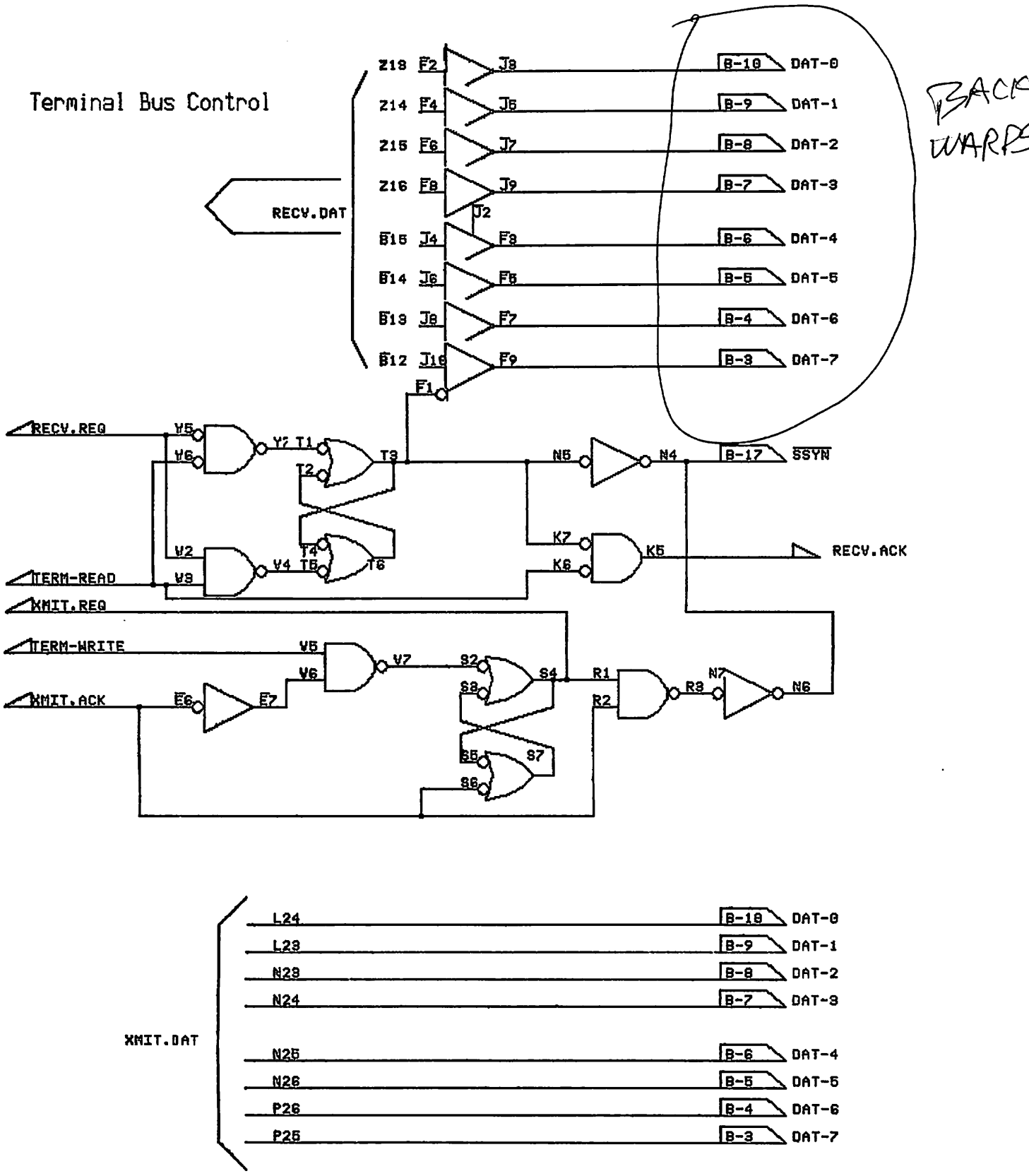
UART LAYOUT

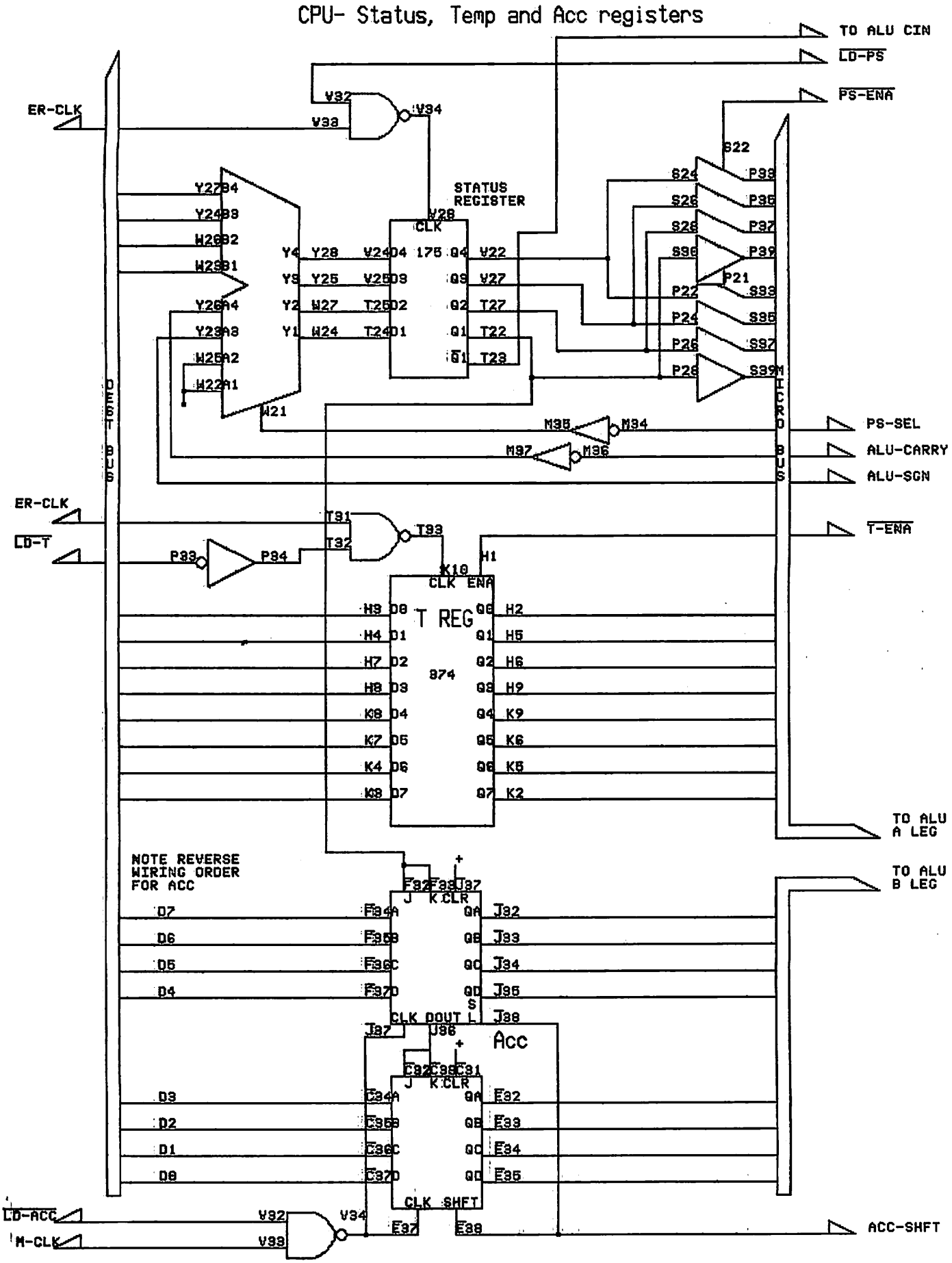
~~X LOOSE ONE SIDE EMPTY FOR POSSIBLE REV W BX~~

Term Interface Selection Logic

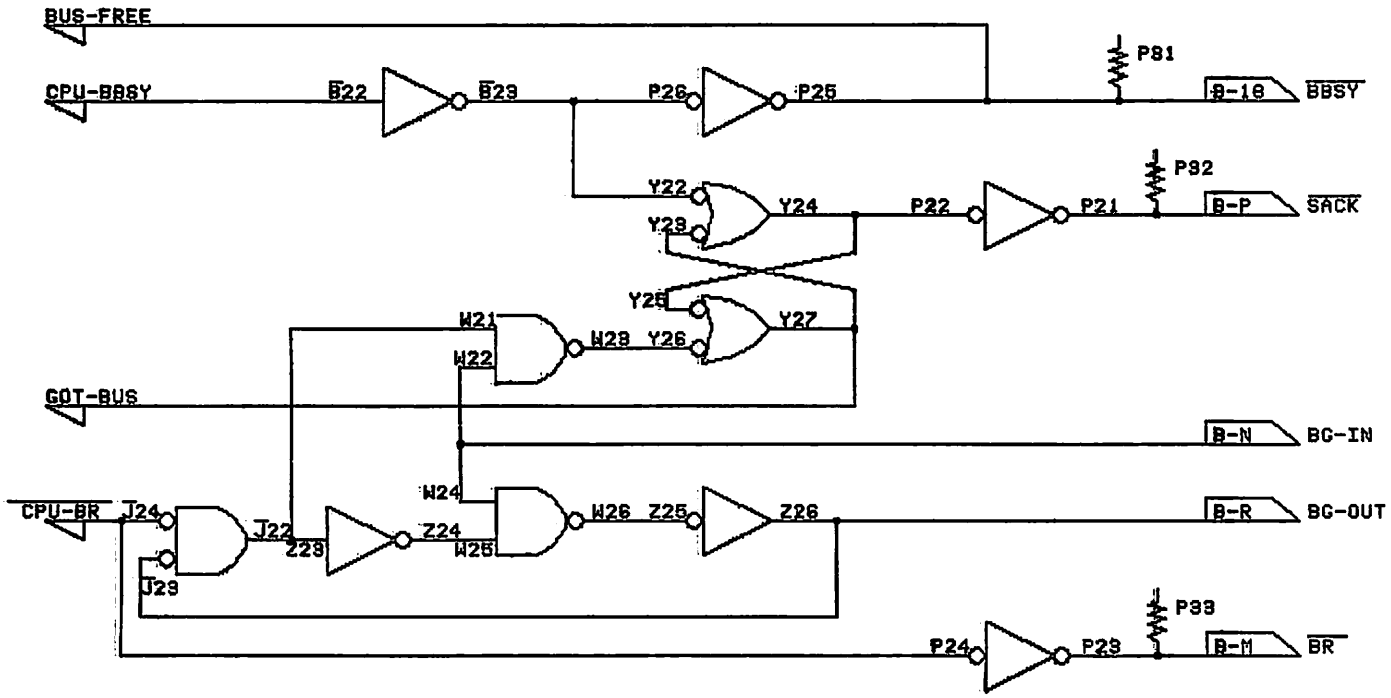


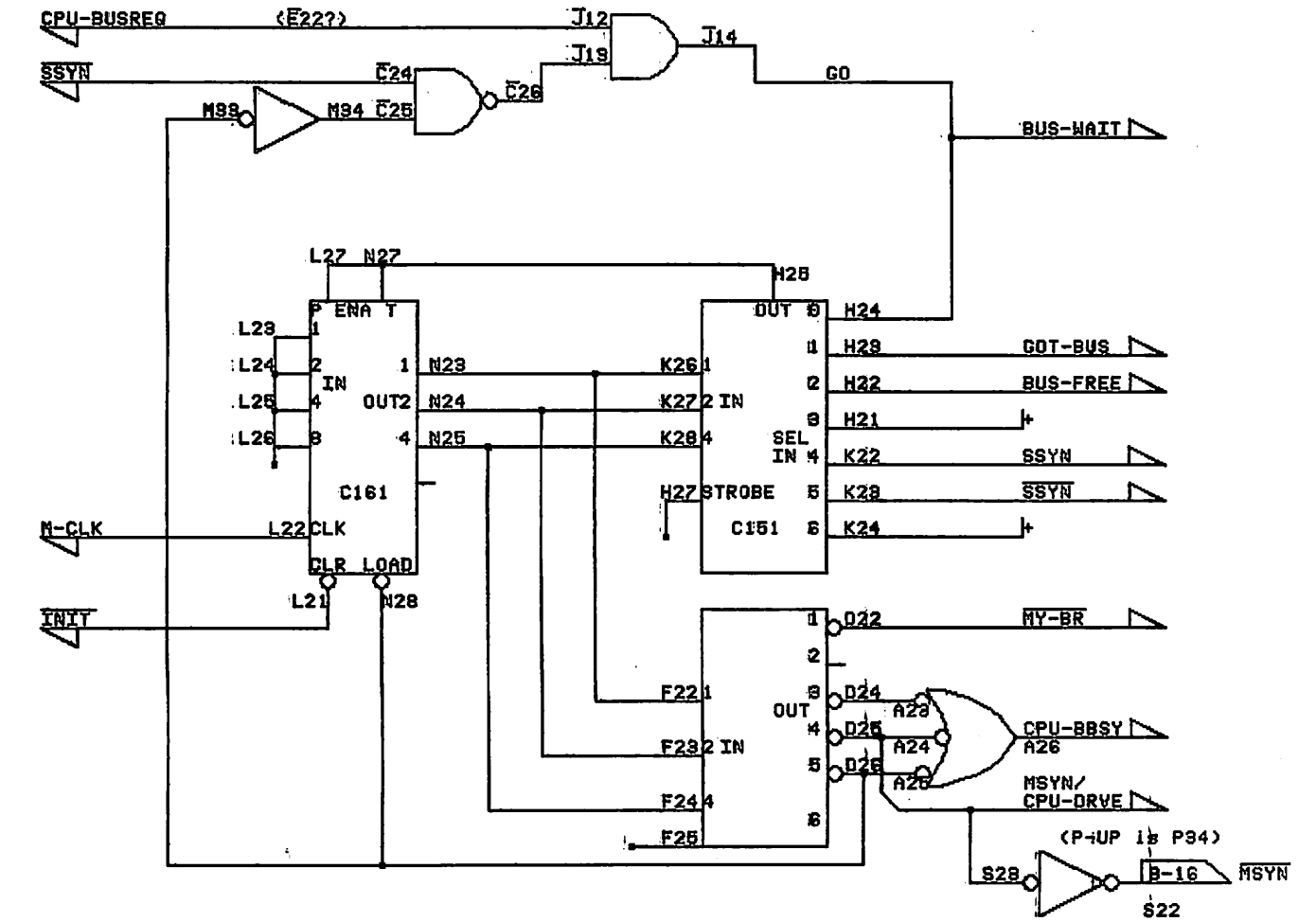
Terminal Bus Control

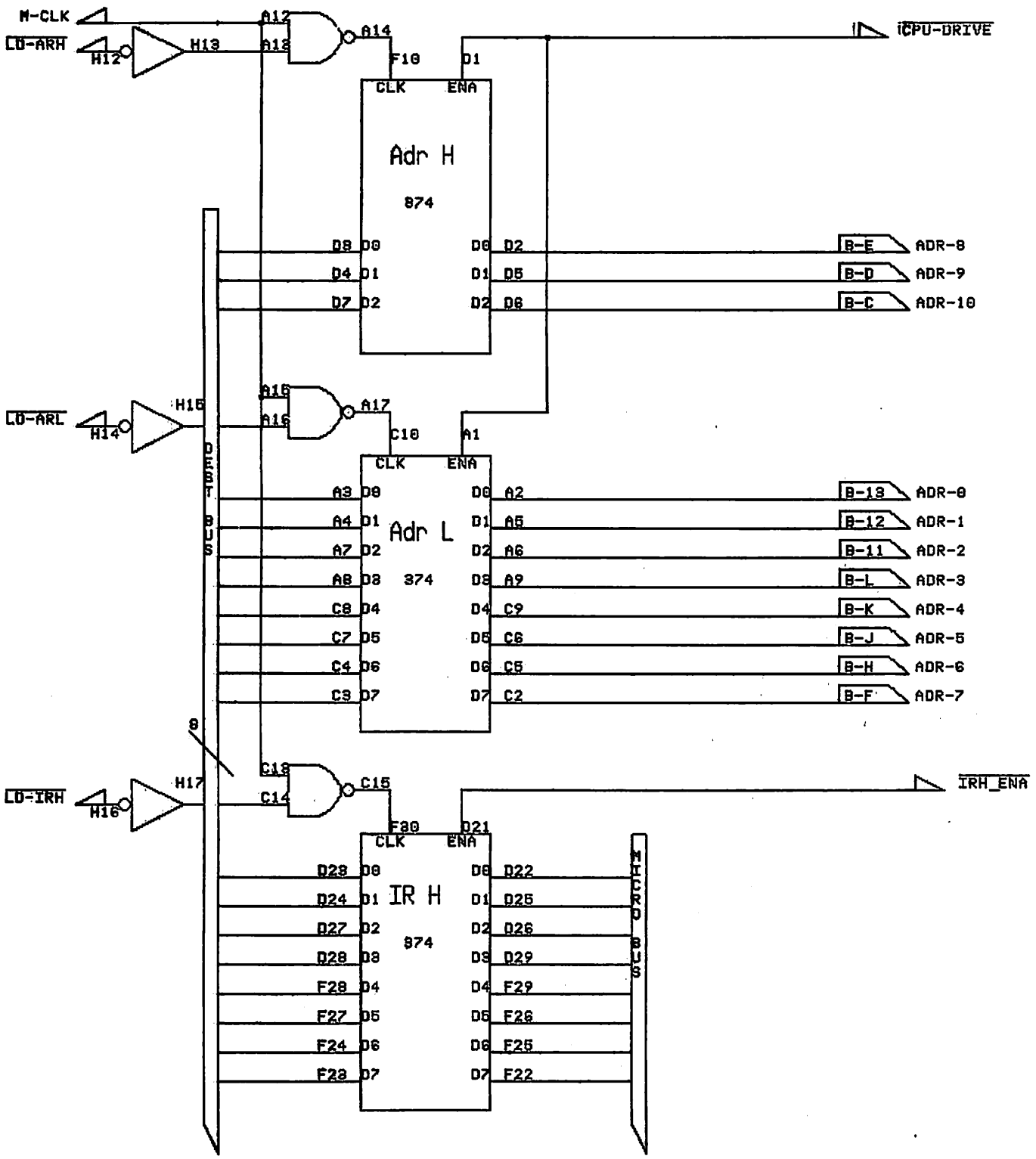



CPU- Status, Temp and Acc registers
TO ALU CIN
LD-PS
PS-ENA
ER-CLK
STATUS REGISTER
PS-SEL
ALU-CARRY
ALU-SGN
T-ENA
LD-T
T REG
TO ALU A LEG
TO ALU B LEG
NOTE REVERSE WIRING ORDER FOR ACC
Acc
LD-ACC
M-CLK
ACC-SHFT

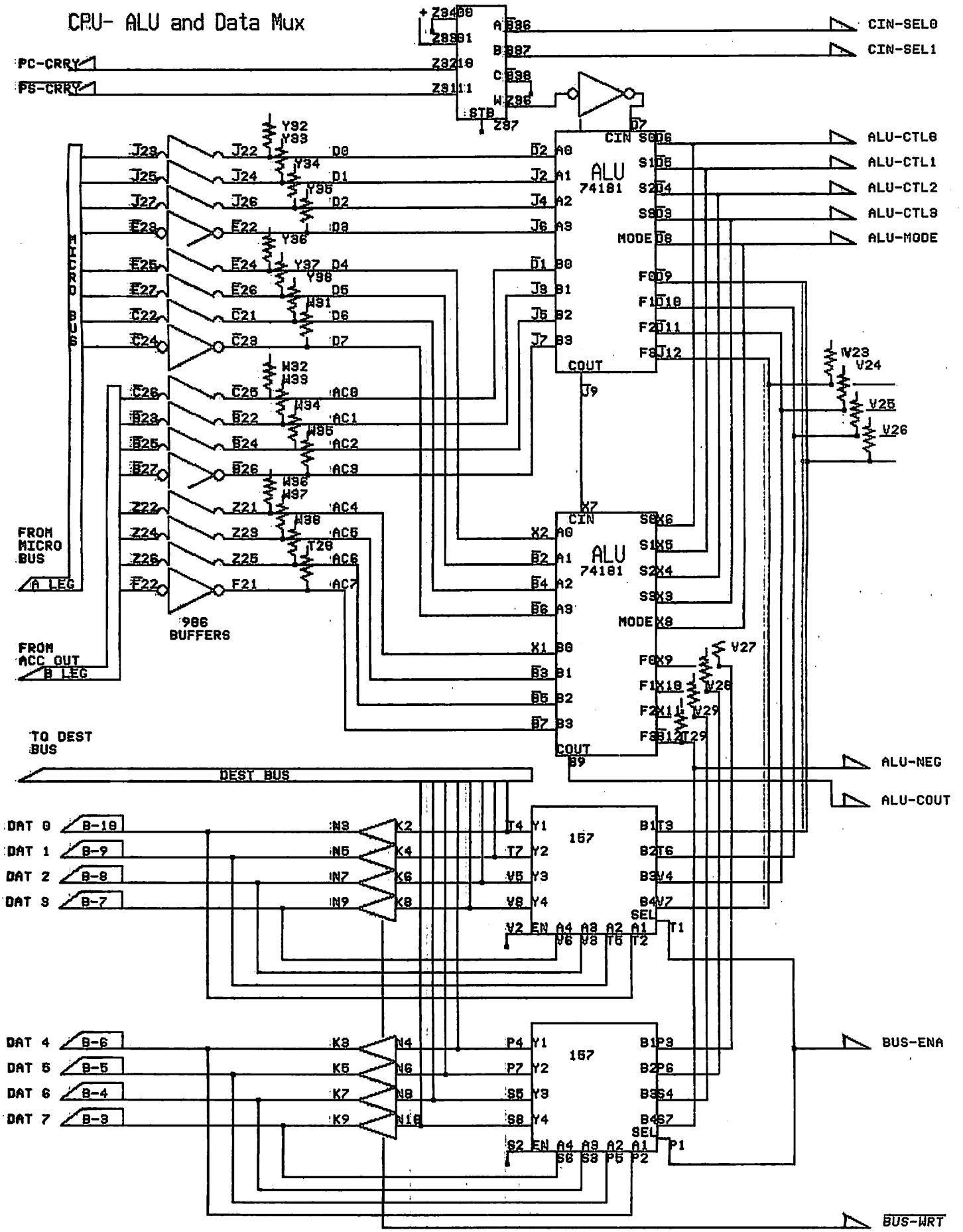
CPU- Bus control logic

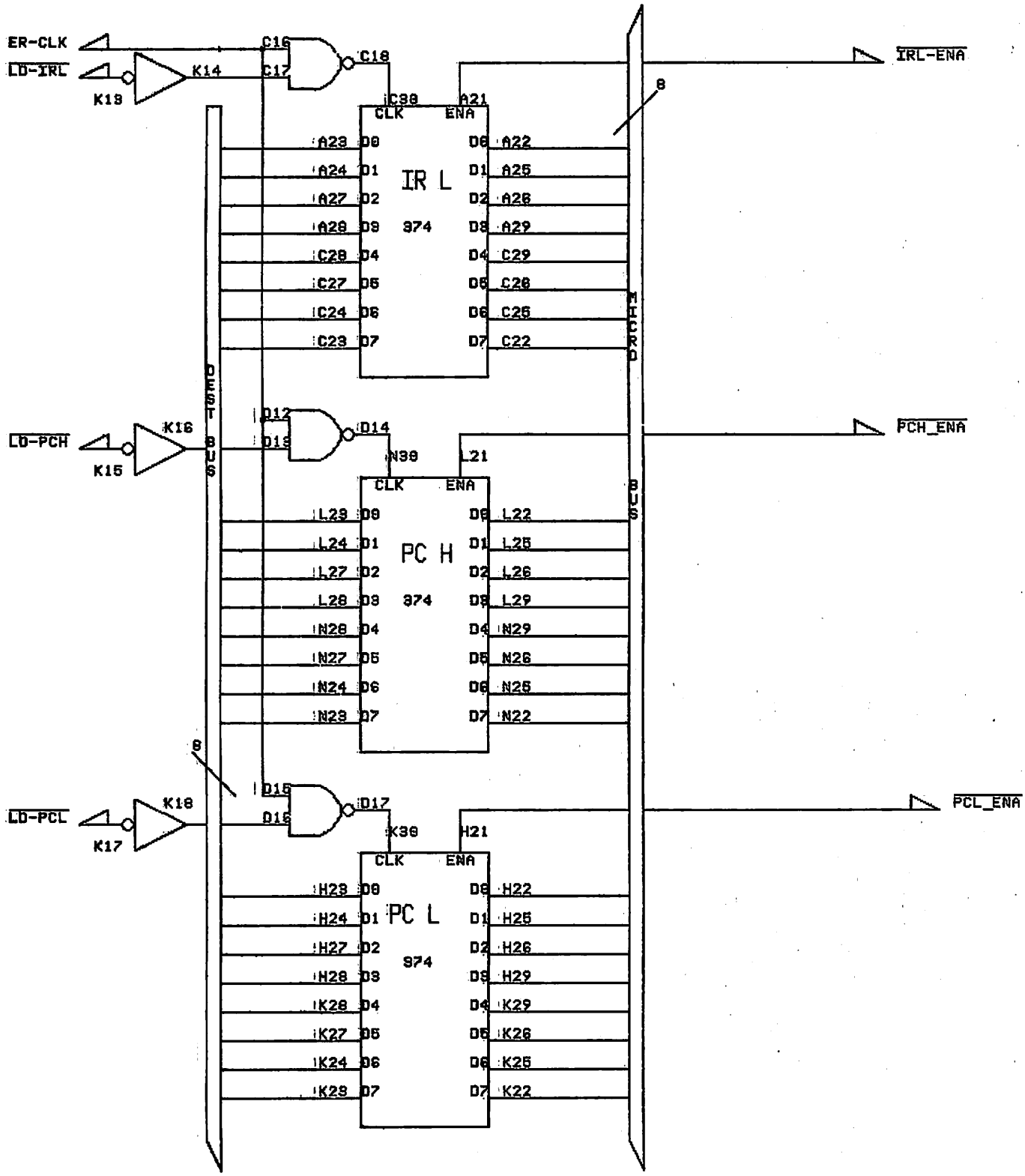






CPU- Address and IRH registers

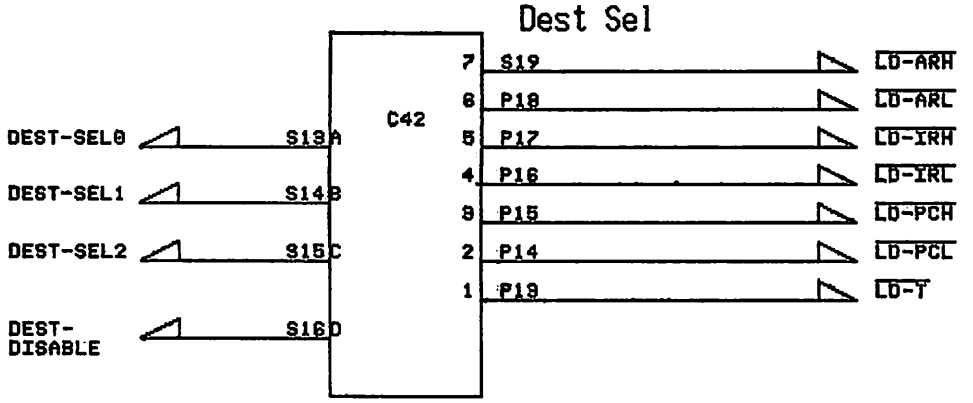

CPU- ALU and Data Mux
PC-CRRY
PS-CRRY
CIN-SEL0
CIN-SEL1
ALU-CTL0
ALU-CTL1
ALU-CTL2
ALU-CTL3
ALU-MODE
ALU
74181
MICRO BUS
FROM MICRO BUS
A LEG
FROM ACC OUT
B LEG
986 BUFFERS
TO DEST BUS
DEST BUS
ALU-NEG
ALU-COUT
BUS-ENA
BUS-WRT
DAT 0
DAT 1
DAT 2
DAT 3
DAT 4
DAT 5
DAT 6
DAT 7
157



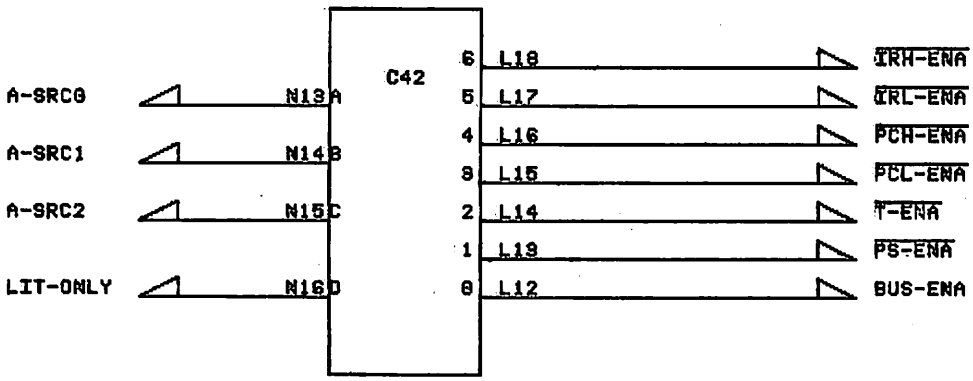
CPU- IRL and PC registers

CPU- Register Selection Logic

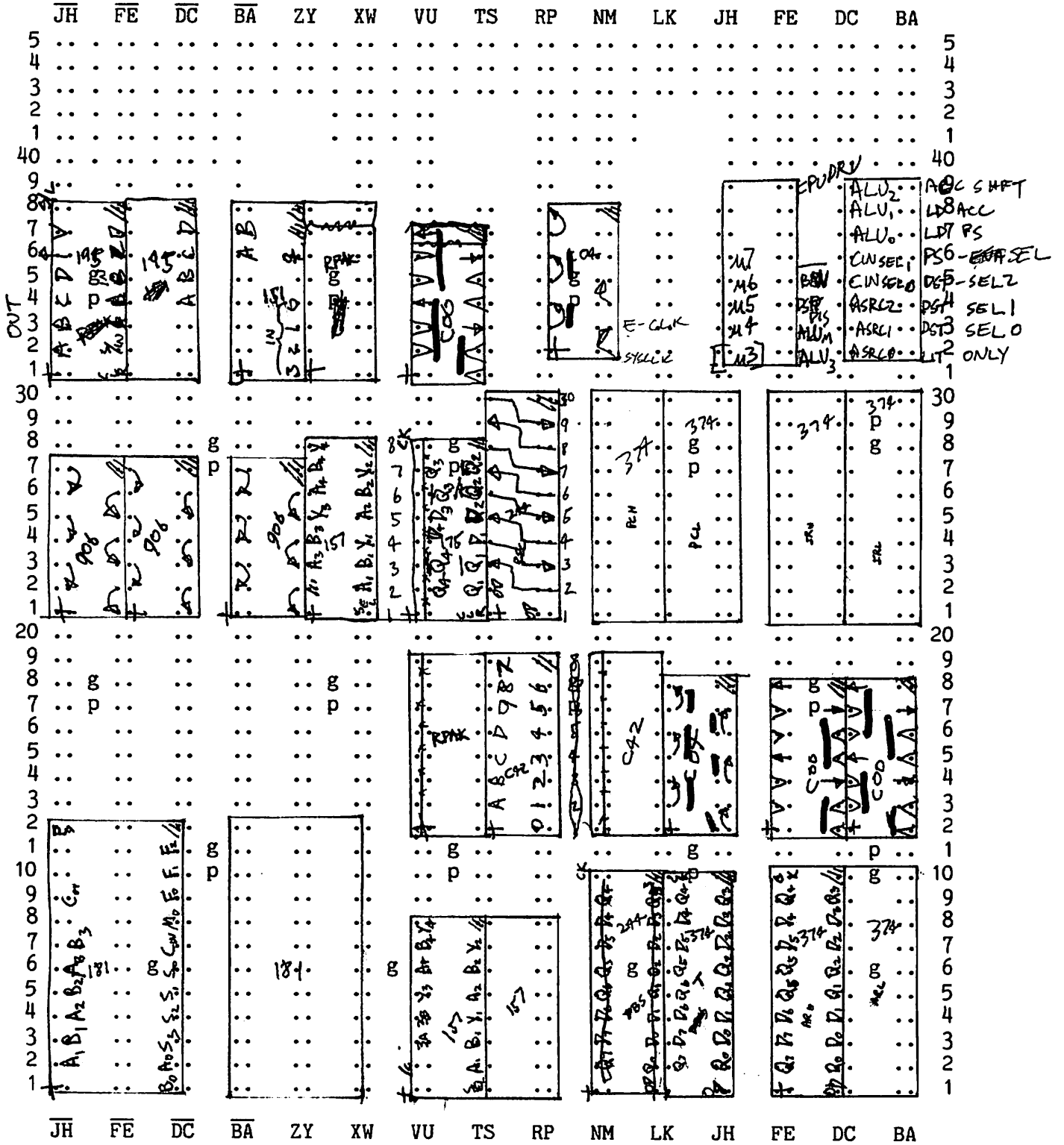
Dest Sel



u_Bus Enable



REGISTER BOARD LAYOUT



D̄	C̄	B̄	Ā	Z	Y	X	W	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C
2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3
6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0							

CONTROL BOARD LAYOUT